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FINAL REPORT

FABRICATION & DEMONSTRATION OF A WDM, ATM, MULTICAST SWITCH

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I. Introduction

The objectives of the project is to build electronic control circuits and photonic devices required to implement an optically transparent WDM, ATM, multicast switch including the functions of cell delineation, virtual channel identifier (VCI) over-writing, cell synchronization, all optical wavelength conversion, cell concentration using fast tunable filters, and optical buffering using WDM optical memories. The switch is a key element for future ultrahigh capacity optical packet networks.

Optical networking technology has well progressed in the past few years. The wavelength-division-multiplexing (WDM) technology prevails all over the world due to the advantages of bringing a huge capacity to existing optical networks without installing new fibers. Recent development on photonic add/drop multiplexers and reconfigurable photonic switches can further facilitate the optical networking. Compared with using electronic switches, they can handle the traffics in a network more conveniently and cost effectively. All-optical-networking concepts are now well accepted by all carriers including even the most conservative carriers like MCI-Worldcom. Recently, due to the growth of internet, the research topics has further moved toward trying to remove the SONET layer out of the optical networks and allowing IP traffics to directly run on top of WDM channels. To do that, one of the most comprehensive solutions is to run packets directly on top photonic packet switches as proposed by European carriers like BT and Alcatel. In facts, the photonic packet/cell switch research has recently become a very important research area. Our work represents one of the few leading research works in the world in this area.

The moment we proposed the work (1993), we have to take care the need of both an OTDM and a WDM networks. The technologies we developed here are useful for either approach. Basically, for each incoming packet/cell from all the optical channels, we need to align them in time before they entering the NxN space switch fabrics. A tunable optical delay line controlled by calculated electrical signals is needed. We may also need to change the information in the packet header before it leaves the switch and goes to the next node. The information could be the VCI in a system using the virtual-channel routing scheme or the packet delay in a burst switching system where the header is ahead of the packet payload. The delay between the header and the payload is changing at each node due to the add-on packet processing delay and the contention resolution delay. Before achieving both of the above functions (tunable delays and header information overwriting) an important function has to be performed and that is the cell or packet delineation function. The work is basically to identify the packet or cell boundaries from a stream of 1-0 optical signals. In a SONET system, the framing function is provided. When we run IP or cells directly on top of an optical channel, the cell or packet boundaries have to be identified.

Currently, there is basically no practical all optical logic devices. It is not hard to understand that electronic logic-and-control circuits have to be employed in this project to perform some critical operations. In our proposed switch, optical transparency is maintained everywhere to keep obtaining the advantages of the bandwidth and bit-rate as well as format independence. On the other hand, the intelligence is provided by the electronics. Since many of the functions at 2.5 Gb/s and above are not commercially available, we have to build them ourselves for the

system demonstration. In this work, we have built 5 control circuit boards running at 2.5 Gb/s. These include two cell delineation circuit boards, two VCI over-writing circuit boards, one pair of cell synchronizer control circuit in one circuit board and one route controller circuit board. We also design and fabricate a 1x2 semiconductor optical amplifier (SOA) broadband space switch. Multiwavelength-signal switching using the fabricated switches is demonstrated. We also build the VCI overwriting and cell synchronization optical systems using both LiNbO3 switches and the fabricated switches. We have completed the interfaces of the optical systems with the control circuit boards and demonstrated the proposed photonic WDM, ATM, Multicast switch at 2.5 Gb/s.

In the project, UMBC is responsible for the optical systems and Polytechnic University (Poly) is responsible for the electronic control systems. There have been many e-mails, phone calls, visits between the two campuses. Since Poly has only a 1 Gb/s testing system and UMBC has a 5Gb/s BER system, many testing works has to be first tuned to 1Gb/s at Poly and moved down to UMBC to be further tuned to 2.5 Gb/s before performing control functions. Poly researchers usually have to stay longer at UMBC to complete interfaces and demonstration. The interaction among graduate students has created a great environment that neither campus can singly provide. Many exciting moments, ideas, problem solving discussions, and conference as well as journal papers have been generated through this process.

In the course of the research works, we have graduated 4 M.S. students, 6 Ph. D. students, and 4 postdoctors (working at Bellcore, Cadence, JDSU, Corning, Tycom, Nortel, and start up companies like Opticallink, Lightcrossing, a cable TV equipment company, SVAC, Agility, Chorumtech, Lucent, Nokia, ...etc). We have published 12 Journal papers, 60 conference papers, and obtained 1 patent with 3 other patents pending. Our works have drawn a great attention from many different equipment vendors and research organizations including NTT optical networking group, Alcatel, CSELT, New Bridge networks, ...etc.. The PI, Prof. Choa, was also visited by Cisco and invited by 3-Com to visit their head quarter and give an invited talk on our photonic packet switching research. In facts, a consensus has been reached by the optical communication community that fast photonic circuit switches and photonic packet switches will be one of the important directions for next generation optical network researches.

A basic concept has formed after this research work. In an all-optical network cloud, photonic packet switches will be sitting everywhere in the middle of the cloud as backbone switches. Electronic buffered switches will be sitting on the edge of the cloud as edge switches to do format conversions and traffic regulation. Bursty traffics will be mostly buffered at the edge of the all-optical network and packets go to the same network address will be packed to a large cell with a fixed length before send into the all-optical network. Inside the all-optical network, the backbone switches will handle fixed size cells all optically with fiber delay lines or loop memories. Since the traffics are relatively regulated, the buffer size requirement is more relaxed. Such a concept is now starting to be accepted by many industrial researchers. As a leading research group in this field, our results can greatly contribute to the optical networking area and have impacts to the next generation Internet (NGI) and the global information infrastructure (GII).

We summarize the developed results in the following:

1. Cell Delineation: To do cell delineation, the tapered and O/E converted signal at 2.5 Gb/s is converted to 16-bit parallel words using a serial/parallel converter and the delineation process is performed at word clock rate, about 155 MHz. The circuits continuously perform CRC calculation following the hunting mode, the presync. mode, and the sync. mode procedure to identify the cell boundary. The cell delineation circuits are using both ECL and GaAs chips on an 8-layer PCB.

2. Virtual Channel Identifier (VCI) Over-Writing: The cell delineation unit provides cell, byte, and bit clock signals to the VCI over-writing unit. A cell size of 64 bytes is used and that including 5-byte guard time, 5-byte head, another 6-byte guard time and the 48-byte information field. The VCI unit generates proper control signals to read data from the VCI table and to control 2x2 optical switches. Packet head overwriting at 2.5 Gb/s has been demonstrated.

3. Cell Synchronization: A programmable delay circuit is used to synchronize the optical cell data with the overwriting data. The required delay is generated as a control word to turn on or off each 1x2 semiconductor optical amplifier (SOA) Y-junction switch like a toggle switch (delay or not delay). The fiber delay length varies from 1/2, 1/4, ... to $1/2^n$ of an ATM cell. The synchronizer accuracy can be as small as $1/2^n$ of one cell period, where n is the number of delay stages. We demonstrated the 1/2, 1/4, and 1/8 packet delays and down to 1/4 bit delays results for an optical packet with 400 ns length at 2.5 Gb/s.

4. 1x2 Semiconductor Optical Amplifier (SOA) Switches: We designed and fabricated Y-junction SOA active/passive waveguide switches and used them for cell synchronization. The switch has a switching speed of 600 picoseconds. The fall time is fast due to the stimulated emission. The rise time is limited by the Auger recombination rate around 1 ns and can be reduced if the switching current is increased. It is capable of switching multiwavelength signals with one switching operation. A word of 64-bit information can be direct to different locations with one fiber, one switch and one switching operation. The extra wavelength domain of photonics can reduce the complexity and cost of interconnects. Such idea is now being explored to be used inside large capacity electronic switches.

5. Wavelength Converters: We use the cross-gain and the cross-phase modulation effects in SOAs to do wavelength conversions. From our discovered "gain decompression effect" we found that we can use either the side injection or the long SOA cavity length to achieve high-speed wavelength conversions. We have made devices for implementing either schemes into our conversion devices and found that the later is more effective. All active Y interferometers and all active Mach-Zender converters with separated injection branches have been fabrication. Conversion results at 5 Gb/s (the speed limit of our BER testing set) were easily achieved.

6. WDM Memories: Fiber loop buffer memories were built. Fixed length packets are injected into the memory and circulated in the loop with different wavelengths. The memory can be

operated as a random access memory in the packet level to store and forward packets not according to the input order. A very small amount of noise starts to accumulate from the 0-level after more than 25 circulation. When the number of wavelength and the circulation times increase, dispersion compensation and S/N ratio recovery in the loop will be required. Similar to the electronic dynamic random access memory (DRAM) case, we can use a refresh circuit to refresh the S/N ratio and write the signals back to the optical memories before they are seriously degraded. Multi-wavelength optical signals were sequentially selected and refreshed in a refreshing unit through an O/E converter, a regeneration circuit, and an E/O converter. A permanent optical fiber loop storage unit can thus be realized.

7. Cell Concentrators Using Fast Tunable Active Filters: Fast tunable filters are used in our work to select packets for output. We have tested our fabricated tunable active filters and used them as wavelength demultiplexers in an 8-wavelength system. It has insertion gain instead insertion loss. The DBR filter is composed of gain, phase, grating, and post-filter gain sections. Error signals for wavelength control and dynamic gain control are extracted from the gain section and feedback to the grating section and the gain section, respectively. The post-filter gain section can be used to switch the output on or off. The central wavelength of the DBR filter can be easily tuned and locked to a desired channel by changing the grating bias current. An 8-channel WDM system with 0.8nm (100GHz) spacing was demonstrated using such filters. A channel rejection ratio of 20 dB was achieved when the average input power of each channel was at -30dBm. The extinction ratio reduced to 15dB when the signal level was increased to -25dBm/channel, due to the gain saturation of the active filter. The saturation power of the device will be improved by using a ridge type waveguides.

8. Route Controllers: The route controller has FIFOs, one for each output port, to keep track of the cells in the loop memory. The information related to an incoming cell is copied to the end of the appropriate output port FIFO based on the R_x value : either to one FIFO for unicast or to the two FIFOs otherwise. The controller selects two cells at the head of each output port FIFO to be sent to the two ports every cell cycle. If a FIFO is empty, an idle cell is output. Dip switches are connected to the control unit to adjust the delay of signals for proper alignment and compensate delays. The unit is done in a FPGA chip which has sufficient pins to allow large numbers of dip switch inputs. Such a large pin count is also necessary to have the capability of adding more inputs and outputs to the unit for more functions. In addition, the chip has large numbers of programmable logic cells so that more complex functions, such as wavelength reservation, can be added when desired.

9. Broadband Optoelectronic Devices to Improve Scalability: After the subsystem demonstration, our works are focused on the scalability of every part of the switch system. Our goals are: 1. Increase the capacity of the all-optical memory one hundred times. 2. Increase the wavelength conversion and the optical space switch wavelength coverage range accordingly. 3. Increase the broadcast-and-select switch size one hundred times. The key to achieve all above goals is to build a new type of material/device that can have extremely broad wavelength tuning range. Two types of gain materials will be studied in this research work: a. The Esaki junction type and, b. The selective-area-growth (SAG) type of gain materials.

a. The Esaki junction type of gain materials: The Esaki-junction type of gain material is composed of N multi-quantum-well (MQW) p-i-n regions each with a different wavelength peak. In between any two of the N MQW p-i-n regions, there is an Esaki junction. An electron will start from the very end n-side, pass through each MQW p-i-n region, tunnel through each Esaki junction, and finally reach the very end p side. One electron will generate N photons, each with different wavelengths. Broadband gain material can thus be achieved.

b. The Selective-Area-Growth (SAG) type of Gain Materials: The SAG type of material uses oxide masks on top of semiconductor wafers to obtain materials with different wavelengths in one single crystal growth. Materials grown in the region with wider oxide coverage, the peak wavelength will shift toward the longer wavelength side. By using different oxide width along the two sides of a waveguide, the material will have different bandgaps along the waveguide. Broadband gain material can thus be achieved.

With the proposed methods, a multiple-quantum-well (MQW) material with a very broad and smooth gain profile of more than 250 nm has been obtained. Using the fabricated material, semiconductor lasers with a very wide tuning range of more than 200 nm From 1280 nm to 1480 nm have been achieved. Wavelength converters that can convert signals across 250 nm wavelength ranges, from 1550 nm to 1300 nm, have also been demonstrated.

10. Long Carrier-Lifetime Low-Crosstalk Materials for Switching and Amplifying: The issues of using semiconductor optical amplifiers (SOAs) as an amplifying material have been their fast gain recovery time. The fast gain recovery time, caused by the short carrier lifetime, produces problems like high channel-crosstalk in a WDM system and high amplified-spontaneous-emission (ASE) noise. In the research work we studied methods to increase carrier lifetime in a broadband SOA. Three different methods were used: a. quasi-indirect bandgap superlattice materials, b. Type II delta-doping materials, and c. SAG exponential gain materials.

a. The Quasi-Indirect Bandgap Superlattice Materials: The materials are composed of multiple layers of direct bandgap and indirect bandgap superlattice materials. For example we can have the GaAs/AlAs (direct/indirect) superlattice on GaAs substrates for shorter wavelength gain materials (700-850 nm), and the AlSb/GaSb (indirect/direct) superlattice on GaSb substrates for long wavelength gain materials (1300-1550 nm). Through band mixing of the X-like and the ?-like bands in these superlattices, the composite superlattice bands will have a carrier lifetime somewhere between a direct bandgap material (~ns) and an indirect bandgap material (~?s). The material gain will be reduced accordingly. However, we can increase the device length to increase the gain similar to the EDFA case. In our research work, we have grown AlAs/GaAs quasi-indirect bandgap superlattice materials and observed materials changing from direct to indirect bandgaps. We grew 2nm/2nm, 5nm/5nm, 8nm/8nm indirect/direct bandgap superlattice materials. We observed that the PL from the 8nm/8nm sample shifted to the shorter wavelength side. We observed much weaker PL signals from the 5nm/5nm sample and shifted to the even shorter wavelength side. We didn't observe any PL from the 2nm/2nm sample. It is believed that the 2nm/2nm sample became an indirect bandgap material. It is highly possible that the carrier lifetime has changed from the nanosecond scale to the microsecond scale with the quasi-indirect bandgap material.

b. The Type II Delta-Doping Materials: Using multiple layer of n and p delta doping pairs we can create the nipi structure, which can spatially separate the electrons and holes. Depending on the doping concentration and the separation distance, we can control the carrier recombination lifetime. We have grown hetrostructure gain material with a 100 nm thick 1.3 Q cladding layer on each side and an 80 nm thick 1.55 Q gain layer in the middle. The 1.55 Q material is delta-doped with p and n dopants with a surface concentration of around $5x10^{12}/cm^2$ and a separation of 20 nm. The material shows good PL intensity with a peak shifted to around 1580 nm. It is now sent to another group and waiting for time resolved study results. We expect such a material will have a longer carrier lifetime due to the spatial separation of electrons and holes in the material.

c. The SAG exponential gain materials: The SAG type of gain material provides a gain medium with continuously changing bandgap along the waveguide. With a constant current injection, the carrier distribution along the waveguide is exponentially increased from the larger bandgap side to the small bandgap side. If multi-channel WDM signals are injected from the shorted wavelength side of the waveguide, they will see an exponentially increased gain before them. The gain will not saturate in this case. No crosstalk will happen. We have tried such an experiment and found indeed that there is no crosstalk between WDM channels when we inject signals in this way. We observe serious crosstalk when we inject WDM signals from the opposite side. Such results have been predicted in two of our previous theoretical papers. The opposite direction injection will make the WDM signals see an exponentially decreased gain along the waveguide and it makes perfect ultra-high speed all-optical wavelength conversion, switching, and logic devices.

II. DETAILED RESEARCH RESULTS OF THE WDM, ATM, MULTICAST SWITCH:

1. An Overview of The 3M Switch

The WDM ATM Multicast (3M) switch is an optically transparent ATM switch proposed by us. It combines the superiority of WDM and ATM techniques to provide a flexible and high-capacity switching function for the high-speed network. It takes advantage of photonics in large bandwidth and electronics in control and storage. The switch has a two-layer structure, where the ATM cell and its electrically converted routing header are split at the input port and then travel in parallel through an optical cell switching network and an electrical header processing and control network. The interconnection complexity of a switch fabric can be greatly reduced from $O(N^2)$ to O(N) by using the broadcasting and select scheme of WDM.

Figure 1 shows the architecture of an enhanced N ? N 3M switch, where each port carries optical ATM cells at 2.5 Gb/s. The incoming data is split into two identical paths in each input port. One path remains in the optical domain through the switch, and the other is converted to an electronic format for header processing. Header processing performs table lookup and determines to which output ports the cells are routed. An electronic central controller, enclosed by a dashed line in Figure 1 performs the functions, such as cell delineation, VCI-overwrite

controller, cell synchronization controller, and route controller. The first three are implemented in the in the front-end processor. The route controller is being implemented to control the optical switch fabric, including wavelength converters, tunable filters, and a WDM optical memory. In the optical path side, after the synchronization and VCI overwriting, cells from each port will be wavelength-converted to different ?$_i$ (i=1,...,N) by N wavelength converters and sent to the WDM buffer memories to wait to be selected by the optical concentrators at the corresponding output ports. The WDM memories perform all optical buffering to temporarily store contented optical cells until the output port is available. These operations complete the switching and contention resolution functions of a share-memory switch. The final wavelength converter stage will shift cells to their preferred wavelengths.

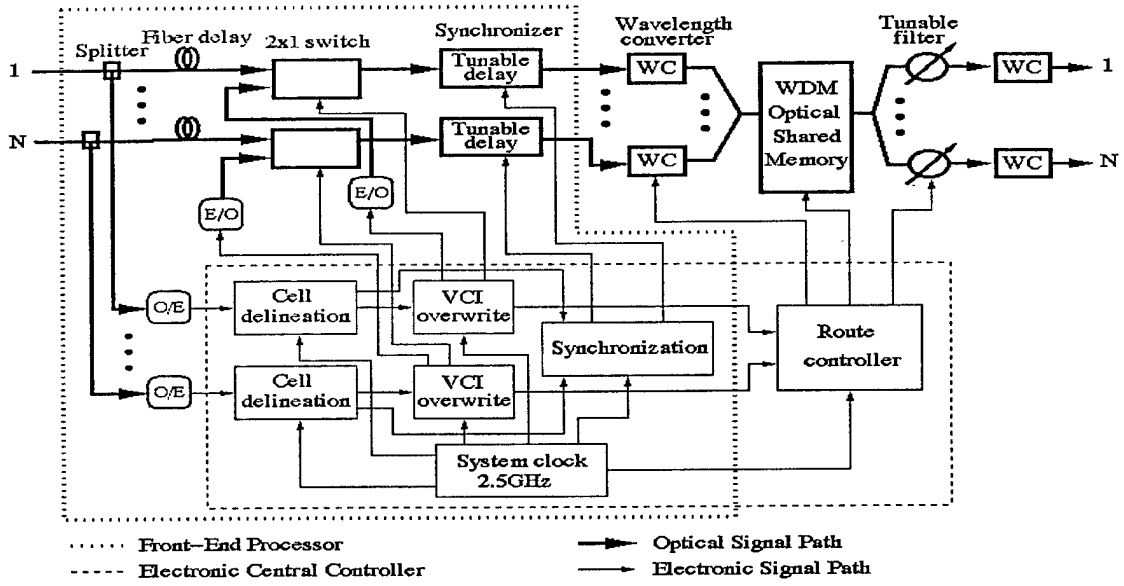


Figure 1 Architecture of the WDM ATM Multicast (3M) Switch

2. Cell Delineation Unit

As shown in Figure 1, the optical cell stream is taped from each input line, converted to electronic format, and sent to the cell delineation unit. Cell delineation is a process used to identify the cell boundaries so that the incoming data stream can be further processed at the cell level by the following units, such as VCI-overwrite.

To search for the cell boundary, we adopted the standardized mechanism, checking of header error code (HEC). It takes advantage of the inherent Cyclic Redundancy Check (CRC) coding correlation between the cell header to be protected (the first 4 bytes) and HEC byte (the 5th byte of cell header). Initially, cell boundary is arbitrarily assumed and checked by performing a polynomial division bit by bit in the HUNT state. If the remainder (i.e., syndrome) for a complete calculation is zero, then this boundary is assumed to be correct. Otherwise, shift a bit

from the data stream and repeat the procedure until the syndrome is zero. Once a cell boundary is primarily found, it has to be confirmed cell by cell for eight consecutive times in the PRESYNC state before the cell boundary is determined to be found. It then goes to the SYNC state. Once in the SYNC state, the cell boundary is claimed to be lost when seven consecutive mismatches occur. As a result, the above procedure for cell delineation will start all over again (from the HUNT state).

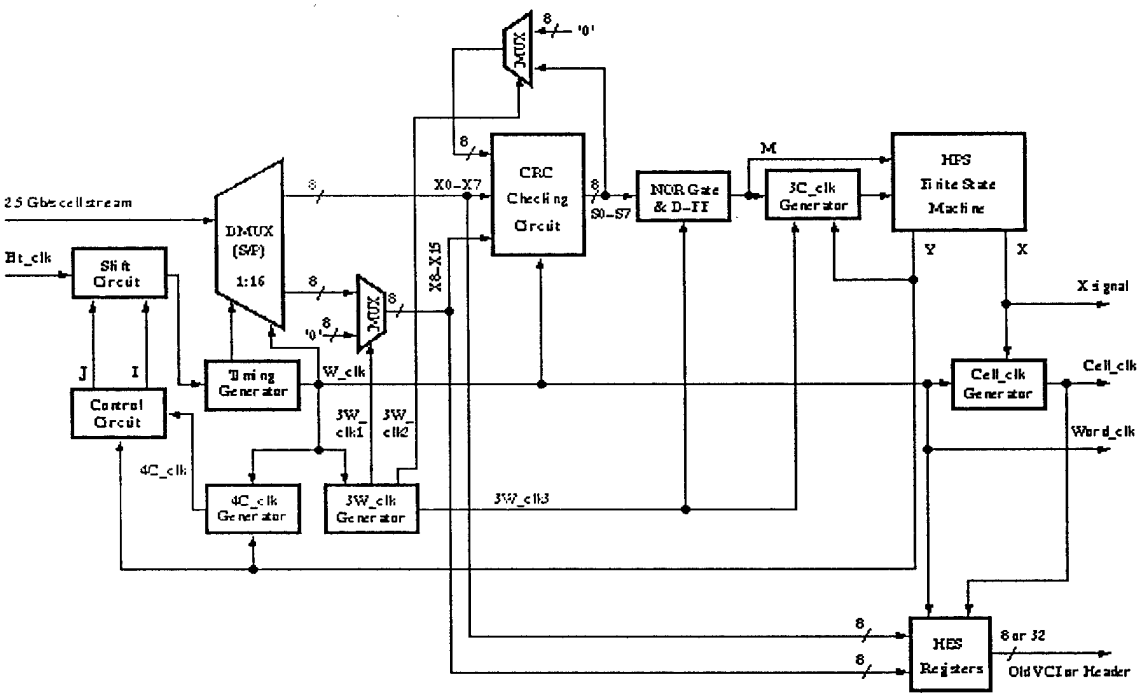


Figure 2 Block Diagram of the Cell Delineation Unit

As shown in Figure 2, in order to relax the high-speed circuit requirement, the serial bit stream (2.5 Gb/s) is first converted to 16-bit parallel words (155 Mb/s) through a serial to parallel converter. A 16-bit parallel format of CRC checking circuit is used to perform polynomial division and the syndrome is checked every three-word clock cycle. A HPS (HUNT, PRESYNC, and SYNC) finite state machine is used to perform the state transition between HUNT, PRESYNC, and SYNC states, as mentioned above. If a syndrome equals zero, then the finite state machine goes to PRESYNC from HUNT state and disables a set of control and shift circuits by a signal Y. Otherwise, the finite state machine informs the control and shift circuits to inhibit a bit and a byte every three cell clock cycle. Once the cell boundary is confirmed, the state machine goes to SYNC state and sends a signal X to create a cell clock, which indicates to the location of the cell boundary that is found. The cell clock and signal X are passed to the VCI-overwrite unit together with the old VPI/VCI and the word clock.

3. VCI-overwrite Unit

Once cell boundaries are recognized and confirmed by the cell delineation unit, the state machine moves to the SYNC state and enables the VCI-overwrite unit with the cell clock and signal X, as shown in Fig. 3. The main function of this unit is to overwrite the VPI/VCI field of the incoming cell header in the optical domain. The VCI-overwrite unit performs the table lookup in the electronic domain, converts the new VPI/VCI to optical format, and replace the old values by using a 2 ? 1 optical switch. The challenge is how to handle this high-speed overwriting because each bit is only 400ps at the bit rate of 2.5 Gb/s. We solve it by (a) replacing the whole cell header instead of just only the VPI/VCI fields, and (b) using electronic variable delay lines (programmable delay) to compensate for the time difference between the old header and the new header.

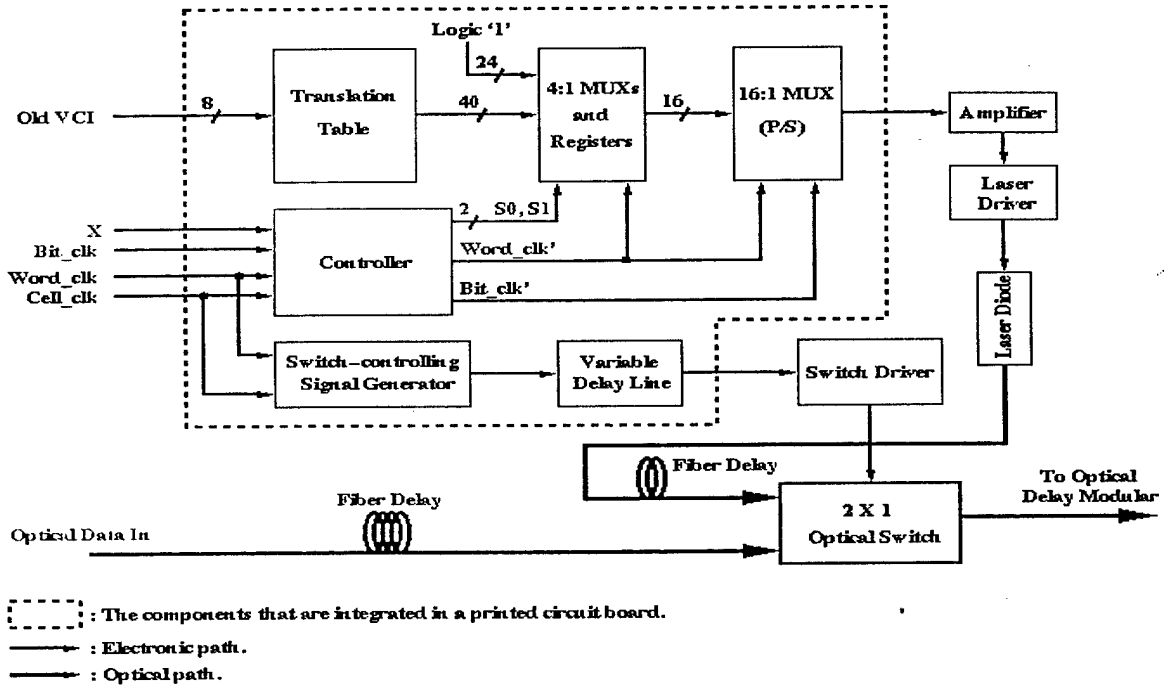


Figure 3 Block Diagram of the VCI-overwrite Unit

As shown in Figure 3, the new header is obtained by table lookup and then converted to serial format by a parallel to serial converter. Then, it is used to control a laser driver to drive a DFB laser diode that generates the cell header in the optical domain. The new header replaces the old one using a 2 ? 1 optical switch that is controlled by a switch-controlling signal generator with 6 bytes of pulse in every cell time slot. The successfully overwritten cells are sent to fiber delay lines in the cell synchronization unit.

4. Cell Synchronization Unit

The cell synchronization unit is used to optically align cells from different inputs to the extent of 1/4 bit (100 ps or 2 cm optical delay line at 2.5 Gb/s) before they are further sent to the switch fabric. Because of this timing requirement, we divided our control system into two parts. A coarse adjustment circuit is used to control the first nine stages of the optical delay element up to 1 bit, and a fine adjustment circuit is used to control the last two stages up to 1/4 bit. Each stage of the optical delay element consists of a splitter, a combiner, two semiconductor optical amplifier (SOA) gates, and a different length of fiber delay line $T/2^n$ (where T is one cell time and n is from 1 to 11). Figure 4 shows the functional block diagram of this unit.

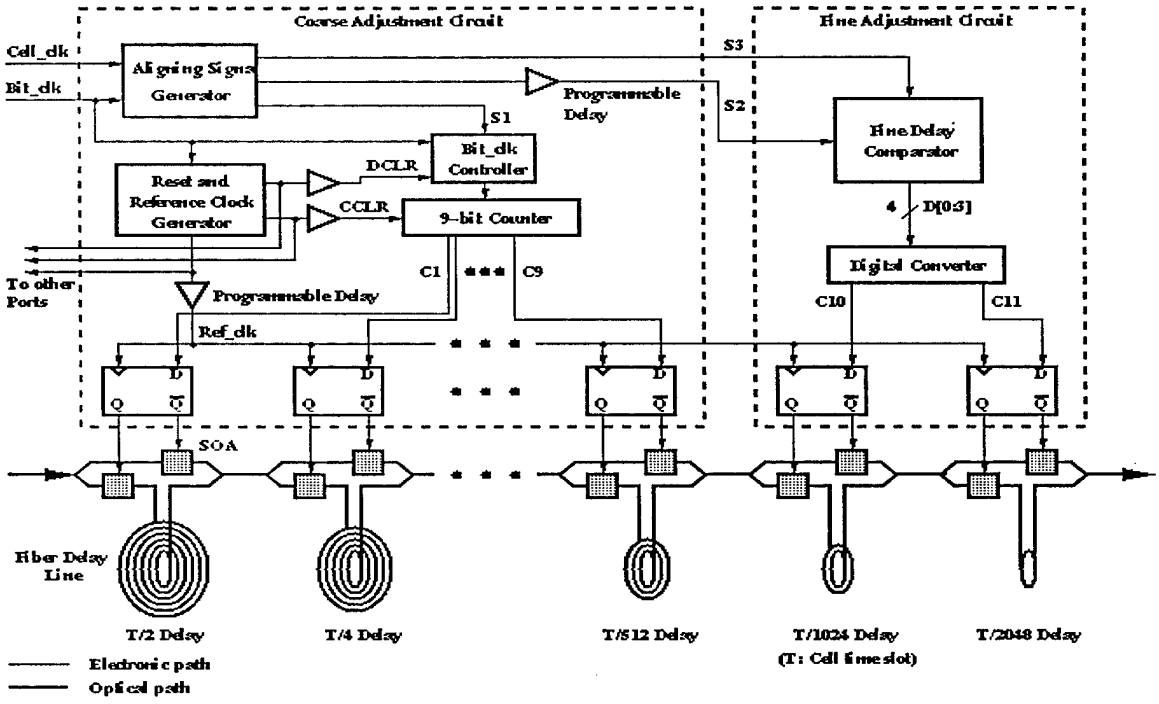


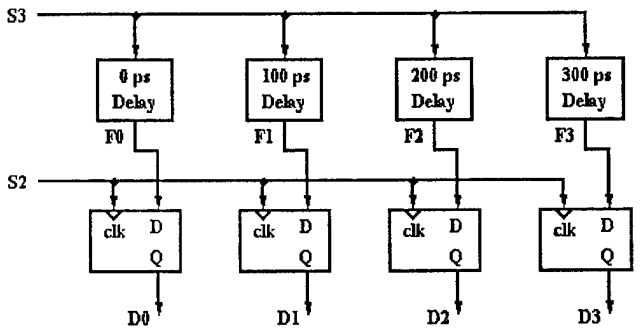
Figure 4 Block Diagram of the Cell Synchronization Unit

As mentioned before, the cell clock generated in the cell delineation unit can be used to indicate the real location of the cell boundary. Therefore, by comparing this cell clock to a reference clock generated by the system, a 9-bit digitized timing difference (up to one bit level) can be obtained by using a 9-bit counter in the coarse adjustment circuit. Each binary digit (C1 to C9) is used to control the switching at the two SOA gates, to determine if each cell passes or does not pass the fiber delay line, in one of the first nine stages of the optical delay system.

However, to identify the timing difference for less than one bit is challenging. A novel sampling technique is adopted to avoid using a 10-GHz clock to adjust the phase down to 100 ps. Figure 6 shows the circuit, which adjusts signal S3 (related to cell clock) into four kinds of phase differences by delaying 0, 1/4 bit (100 ps), 1/2 bit (200 ps) and 3/4 bit (300 ps). Signal S2 (related to bit clock) is used to sample these four different phase-delayed signals to get four sampled signals, [D0, D1, D2, D3]. By converting them into two digits, C10 and C11, according

to the conversion table shown in Figure 5, we can use them to control the SOA gates of the last two stages of the optical delay system.

With different combinations of C1 to C11, all stages of optical delay elements are tuned to the desired delay needed to compensate and align the phase of incoming cells. For example with [C1, C2, ..., C11] = [1, 0, 1, 0, 0, 0, 0, 0, 0, 0, 1], a total delay of $T/2 + T/2^3 + T/2^{11}$ (the last term is 1/4 bit) , is added by the cell synchronization unit.



(a) Fine Delay Comparator

C10	C11	D0 (0ps)	D1 (100ps)	D2 (200ps)	D3 (300ps)
0	0	0	0	0	0
0	0	1	0	0	0
0	1	1	1	0	0
1	0	1	1	1	0
1	1	1	1	1	1

(b) Conversion table between [C10,C11] and [D0,D1,D2,D3]

Figure 5 Fine Delay Comparator and a Table Conversion

5. Implementation and Testing of The 3 Units:

In this section, we described in detail the architectures of three basic units of the photonic ATM front-end processor. Their implementation and testing results are described in this section.

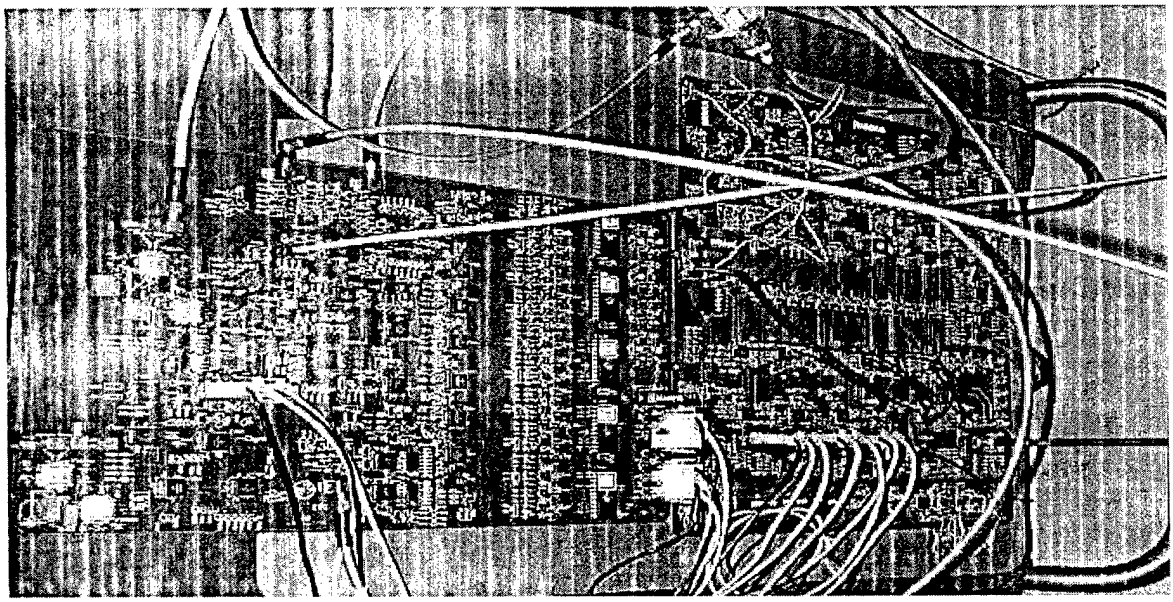
5.1 Implementation

In order to implement the photonic front-end processor operating at 2.5 Gb/s, we use off-shelf ECL or GaAs chips to implement the three basic units in three printed circuit boards (PCBs). We used Mentor Graphics's Design Architech to design the circuits and Quicksim II to simulate and check the circuits. We then used Borad Station, including Librarian, Package, Layout, and Fablink, to design the PCBs. Since the operation frequency of the PCBs is at 2.5 GHz, the wiring layout is done manually to ensure the delay skew is minimized. Note that each

bit has only 400 ps. These PCBs are fabricated by Multilayer Technology. The boards were first tested at 1 Gb/s at Polytechnic University due to the speed limitation of the instruments. They were then integrated with optical subsystems at the University of Maryland, Baltimore County, and tested to function correctly at 2.5 Gb/s.

5.2 Cell Delineation Unit Board

Figure 6 shows the PCBs of the cell delineation and VCI-overwrite units. The components we used are mostly Motorola's ECLinPs Family ICs and small quantities of NEL's SST ECL Logic ICs and GaAs ICs. The NEL's GaAs ICs outperforms all ECL ICs in speed characteristic, but are more expensive. They are only used in the shift circuit of the feedback part, as shown in Figure 3 (file: cl.eps), where we need to inhibit a bit from bit_clk and shift a bit in case the assumed cell boundary is incorrect. In addition, a Vitesse's 16-bit demultiplexer (VS8062) is used to perform serial to parallel conversions. This chip converts a 2.5 Gb/s serial bit stream to 16-bit parallel words at 155 Mb/s. The advantages of parallel conversion are to reduce the number of high-speed components and implementation costs, and to simplify the design and testing of circuits.



VCI-Overwrite board Cell Delineation board

Figure 6 The PCBs of the Cell Delineation and VCI-overwrite Units

In addition to selecting suitable chips to meet our high-speed requirement, the high quality of the PCB material (Getek) is used to meet the high-speed requirement. The impedance of the interconnection wires is 50 ohms. The PCB has 8 layers and its the physical size is 15 ? 13 inches. Figure 6 summarizes the characteristics of these PCBs.

5.3 Electronic Controller of VCI-overwrite Unit Board

We use a few CMOS chips, Atmel's EPROMs (AT27C256R), on this PCB to store the translation table information. Instead of using RAM (random-access memories) chips with a microprocessor to update the table dynamically, the EPROM chips are used to simply the design. In addition, a Vitesse's 16-bit multiplexer (VS8061) was used to perform the parallel to serial conversion for the cell headers, which are further converted to optical format to replace the old header values. The characteristics of board are shown in Figure 7.

Board Name	Cell Delineation	VCI–Overwriting	Cell Synchronization
Size (inch)	15 x 13	15 x 10	15 x 20
Number of Layers	8	7	10
Material	Getek	Getek	Getek
Maximum Operation Speed	2.5 Gb/s	2.5 Gb/s	2.5 Gb/s
Power (watt)	40	25	41
Number of IC	95	94	61 + 36/N †
Components	Motorola's ECLinPS Family NEL GaAs IC NEL SST ECL Logic IC Vitesse's MUX/DMUX GaAs IC Atmel's AT27C256R EPROM		

† There are 36 chips in Reset and Reference Clock Generator that are shared by all ports (N).

Figure 7 Summary of the Printed Circuit Boards

5.4 Electronic Controller of Cell Synchronization Unit Board

Because of the need to align the incoming cells to the extent of 1/4 bit, choosing proper components is very crucial. For example, to determine the timing differenceless than one bit between cell and Ref_clk in fine delay comparator, as shown in Figure 6 (file: fcc2.eps), D flip-flops with low setup and hold time are required. Motorola's differential data and clock D flip-flop (MC10EL52) meets this requirement with zero setup time and 50 ps hold time. In addition, we used several Motorola's programmable delay chips (MC10E195) to adjust and compensate for the timing of several signals in the coarse and fine adjustment circuits. The typical chip delay is variable and ranges from 1390 ps to 3630 ps with about 20 ps delay step resolution.

The reset and reference clock generator, which is shown in the coarse adjustment circuit in Figure 4, is shared by all input ports in the 3M switch. The PCB, as shown in Figure 8, has 10 layers and its physical size is 15 ? 20 inches. Other characteristics of the board are shown in Figure 7 (file: bsummary2.eps).

All the optical devices and subsystems in the photonic ATM front-end processor, such as SOA gates, laser diode, and 2 ? 1 optical switch, VCI overwriting optical unit, and multistage cell synchronizer optical unit are developed and provided by University of Maryland, Baltimore County. The work is described in the following.

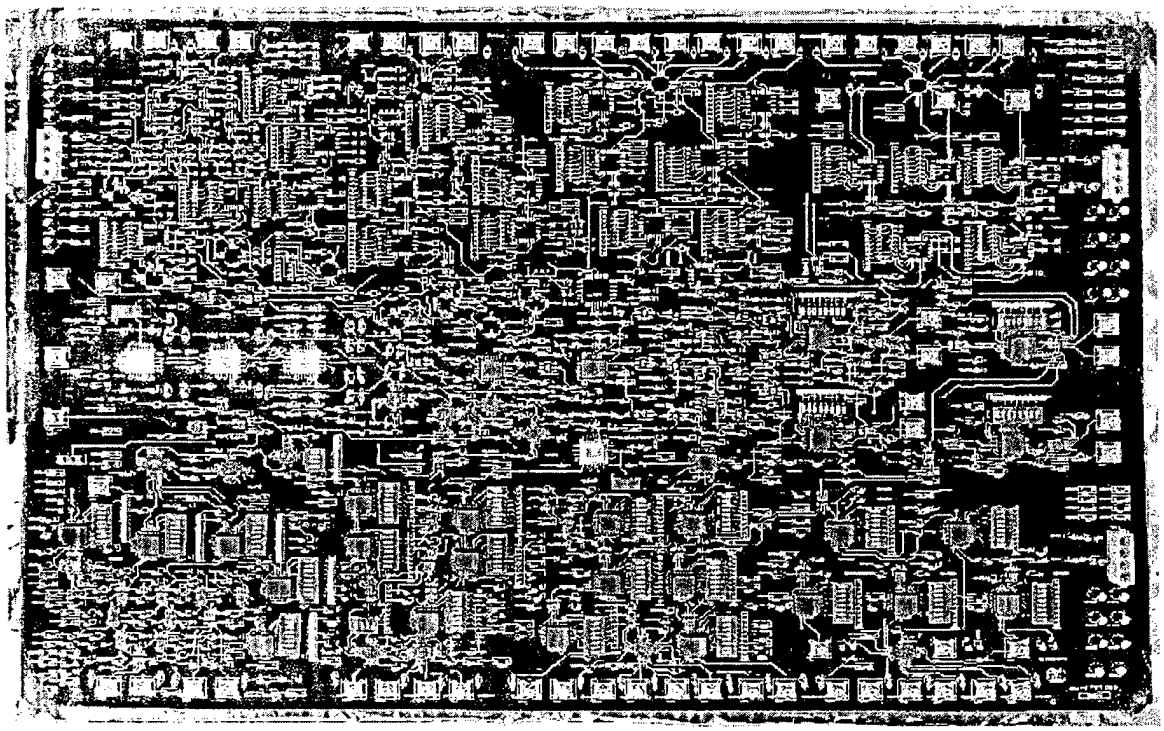


Fig. 8 The Cell Synchronization Circuit Board

6. 1x2 Semiconductor Optical Amplifier (SOA) Switches:

We designed and fabricated Y-junction SOA active/passive waveguide switches and used them for cell synchronization. The switch has a switching speed of 600 picoseconds. The fall time is fast due to the stimulated emission. The rise time is limited by the Auger recombination rate around 1 ns and can be reduced if the switching current is increased. It is capable of switching multiwavelength signals with one switching operation. A word of 64-bit information can be direct to different locations with one fiber, one switch and one switching operation. The extra wavelength domain of photonics can reduce the complexity and cost of interconnects. Such idea is now being explored to be used inside large capacity electronic switches.

In the course of fabricating the integrated 1x2 Y-junction SOA switch we have gone through several generations of devices. Although for each different device generation the performance is always getting improved, the process is effort and material consuming. Fortunately, through the relationship with AT&T Bell Labs. (and later on Lucent Bell Labs.), our projects were firmly

supported by their crystal growth efforts. In the following we report the detailed fabrication processes of the work.

In the first generation Y-junction semiconductor optical amplifier (SOA) gate switches, the active section has a buried heterostructure (BH) and the passive section has a buried rib structure. When we do the BH deep etch we have to protect the passive section with a thick photoresist. Since there is no etching activity in the passive side, the acid is very dense and the etching speed is very fast near the boundary of the active section than that near the center of the active section. The much faster undercutting etching can easily break the waveguide near the active boundary. The yield was low at that moment.

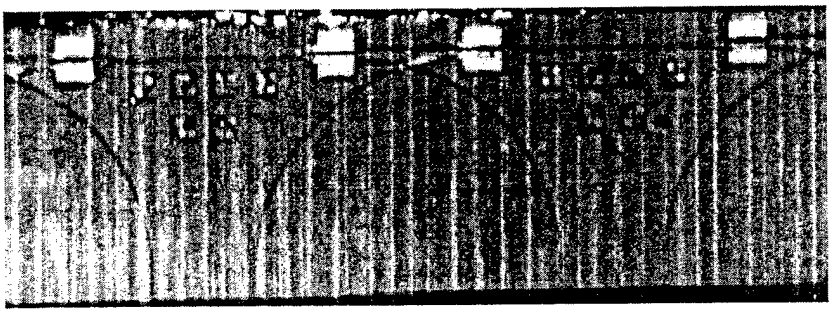


Fig. 9

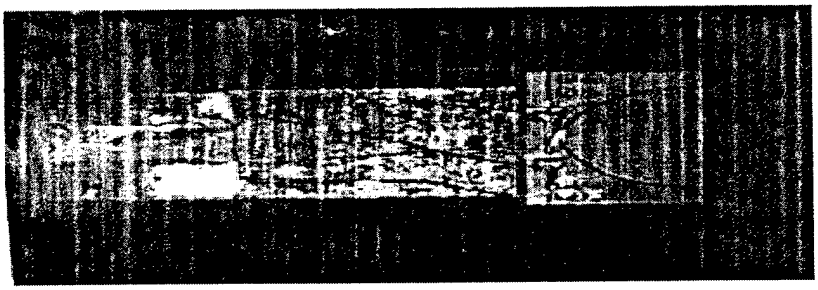


Fig. 10

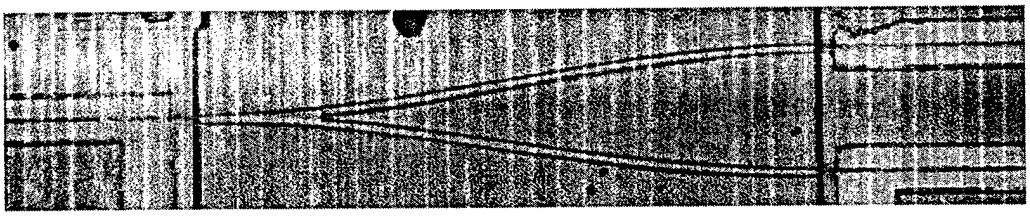


Fig. 11 A fabricated 1x2 SOA gates switch

In our second generation switch and our 10-stage cell synchronizer designs, we have corrected the problem by using masks with wider stripe width near the active/passive junctions. We then completed the fabrication of both the second-generation switches and the first generation of an integarted 10-stage cell synchronizers. An integrated 3-stage cell synchronizer is shown in Fig. 9. A bonded and a chip of the Y-junction SOA gate switch is shown in Fig 10.

In the second generation SOA gate switches we have overcome the non-uniform etching problem and successfully fabricated and demonstrated on/off operations of the switch. However, when we were trying to couple light into fibers from those devices, the distance between waveguides became an issue. The standard distance between waveguides was 508 ?m before. It just changed to 250 ?m and its multiples at that moment. We found later that we can commercially obtain lensed fiber arrays made of silicon v-grooves with standardized (250 ?m) distance between fibers. We also found that to couple light in and out of a semiconductor passive waveguide is extremely difficult. Adding active sections to both the inputs and outputs of a semiconductor chip is very helpful.

Based on the findings, we designed and fabricated our 3rd generation devices as shown in Fig. 11. The distance between the 2 output waveguides are exactly 250 ?m. The active sections on each input and output waveguides are 400 ?m long. We can easily build a multi-stage cell synchronizer using an array of such switches as shown in Fig. 12. The final size of the device can be much smaller than the previous 10-stage cell synchronizers. Packaging can also be simplified from doing 3-side fiber alignment to that of two-side fiber alignment. Fig. 13 shows the switching characteristics of the third generation Y-junction SOA gate switches. The fall time is fast due to the stimulated emission. The rise time is limited by the Auger recombination rate around 1 ns and it can be reduced if the switching current is increased.

Fig. 12 Integrated Cascade multistage 1x2 switches

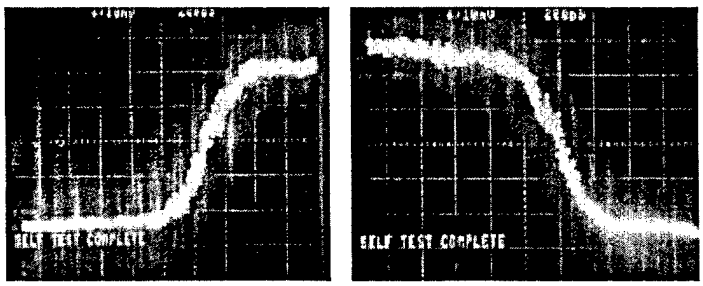


Fig. 13. Switching characteristics of an SOA switch (200 ps/div.).

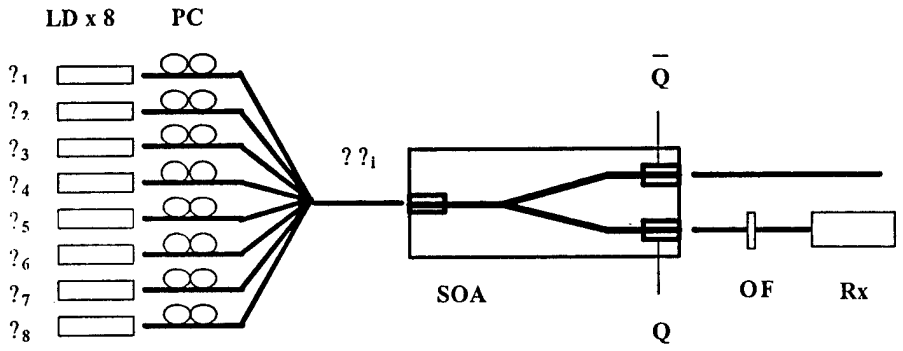


Fig. 14. Experimental setup. PC: polarization controller. OF: optical filter. LD:

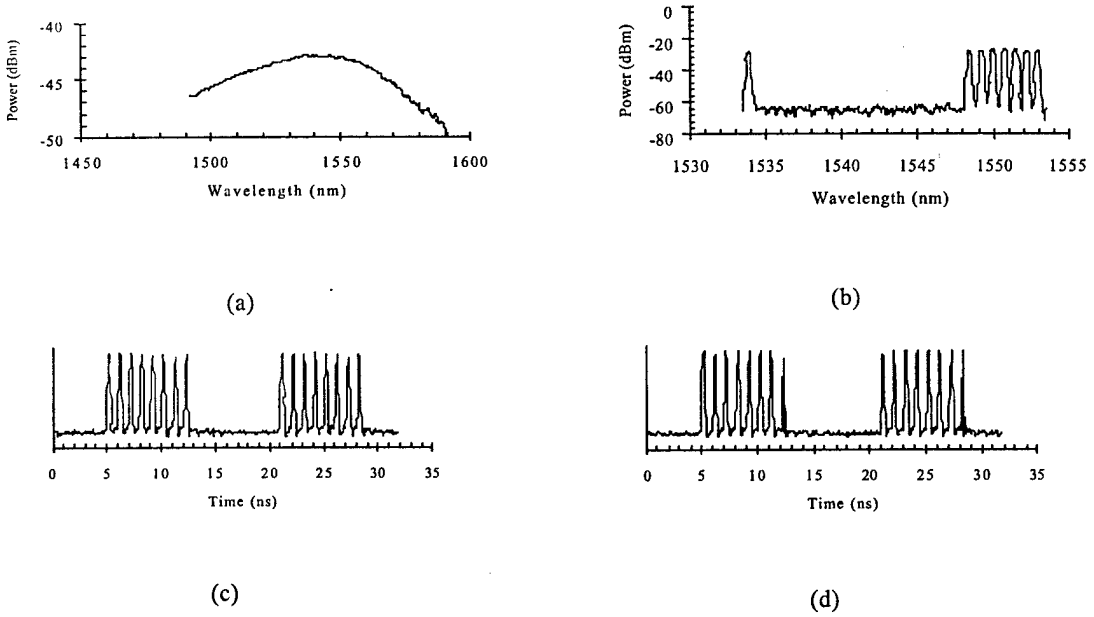


Fig. 15. (a) The SOA gain profile. (b) Multiwavelength signals. (c) Switched "1010" data streams at 1553 nm. (d) Switched "1010" data streams at 1533 nm.

A very interesting application of the photonic space switch is its capability to switch multi-wavelength signals with one single switch and in one switching operation. A word of 64-bit information can be direct to different locations with one fiber, one switch and one switching operation. On the other hand, the same task will require 64 connections and 64 electronic switches on operation. The extra wavelength domain of photonics can greatly reduce the complexity and cost of interconnects. We have experimentally demonstrated a new generation switch, the data block switch, which can direct a full block of parallel data to a desired location. The experiment setup for the data-block switching is shown in Fig. 14. The SOAs have very

broad gain profile covering more than 50 nm as shown in Fig.15 (a). The multi-wavelength light signals, with 7 of them near 1550 nm (separated by 100 GHz spacing) and one at 1553 nm, are coupled into an 8x1 optical coupler and launched into the switch. Fig. 15 (b) shows the multiwavelength spectrum. A tunable filter at the switch output is used to select signals to observe the switching results at each particular wavelength. Fig. 15 (c) and (d) shows the switched "1010" signal streams at 1553 nm and 1533 nm respectively. The "1" and "0" can be clearly identified when the switch is tuned "ON" and the background of the "OFF" state is clear. Very good contrast ratio is obtained and there are very little differences between the received signals and at the two extreme wavelengths.

7. Experimental Results of The Combined Front-End Processor

To validate the design and implementation of the whole front-end system, a series of testing process is necessary. The testing is divided into two parts. One involves the cell delineation and VCI-overwrite units. The other involves only the cell synchronization unit.

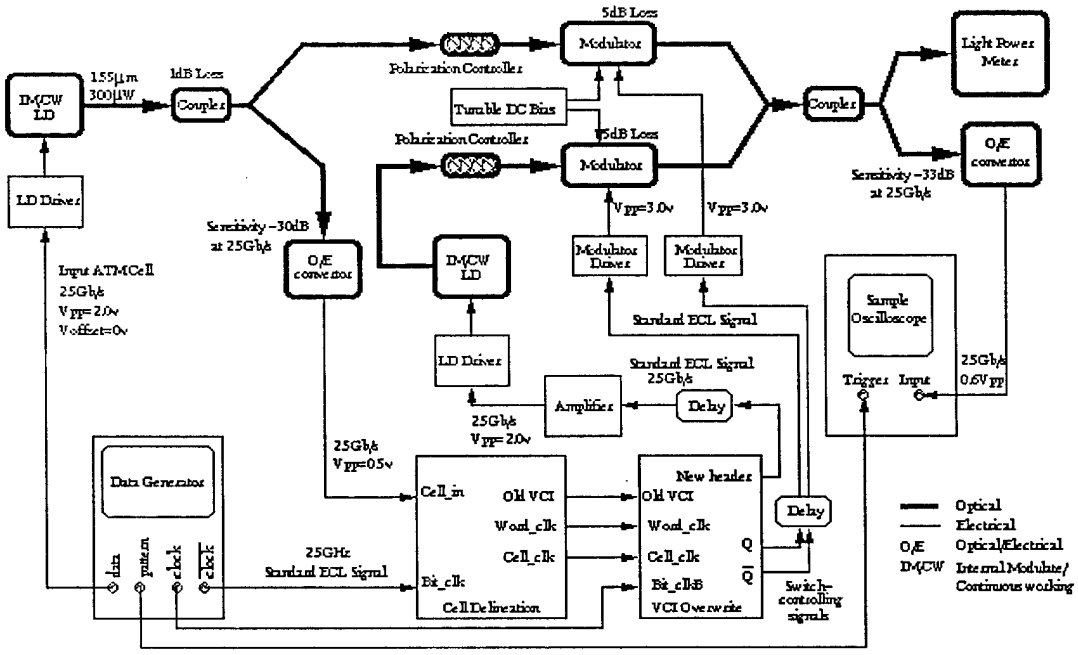


Figure 16 Testing Setup of the Cell Delineation and the VCI-overwrite Units

7.1 Testing of Cell Delineation and VCI-overwrite Unit

We integrated two PCBs (cell delineation and VCI-overwrite units) with the necessary optical devices as shown in Figure 16. A data generator generates the 2.5 GHz Bit_clk and a series of 2.5 Gb/s back-to-back cells. These test cells have 64 bytes with 5 bytes of header, 48 bytes of payload, and two sections of guard times (logic `1'), which are 6 and 5 bytes, respectively, as

shown in Figure 17. The reason for inserting the guard time is to compensate for the slow switching of optical devices, for example, optical tunable filters, which are used in the switch fabric in the 3M switch. To simplify the testing, the test cells have a random payload but an identical cell header pattern, which is {00001010, 11001100, 11101110, 11110000, 10100000}. We assumed that only the third byte (representing VPI/VCI) and fifth byte (HEC byte) are updated in the VCI-overwrite unit.

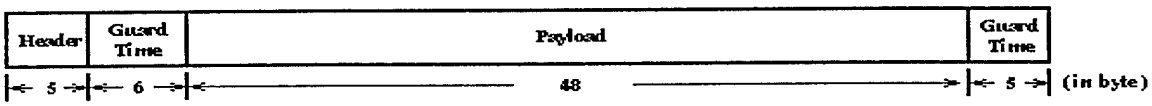


Figure 17 Cell Format in Our Design

Figure 18 shows the testing result of cell delineation and VCI-overwrite units. The new header becomes {00001010, 11001100, 00010001, 11110000, 01110111}, which meets our expectation.

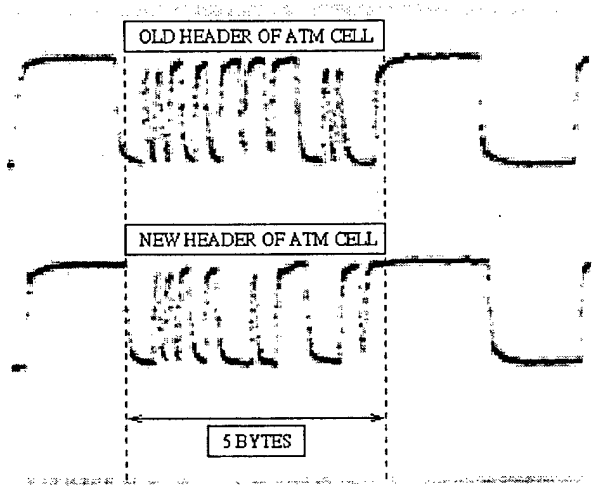


Figure 18 Testing Result of the Cell Delineation and VCI-overwrite Units

7.2 Synchronization Testing of The Cell Unit

We have built a PCB that includes all 11 stages of optical delay elements. The required delay is generated as a control word to turn on or off each 1x2 semiconductor optical amplifier (SOA) Y-junction switch like a toggle switch (delay or not delay). The fiber delay length varies from 1/2, 1/4, ... to $1/2^n$ of an ATM cell. The synchronizer accuracy can be as small as $1/2^n$ of one cell period, where n is the number of delay stages. Fig. 19 demonstrate the 1/8, 1/4, and 1/2 packet delay by using appropriate fiber length for an optical packet with 400 ns length at 2.5 Gb/s. The fiber to fiber insertion loss of the SOA switch is currently at 5 dB. It achieved a very good contrast.

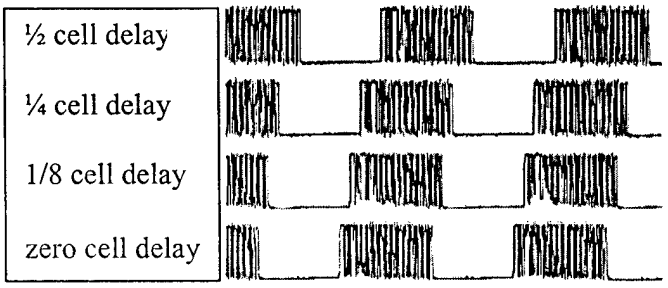
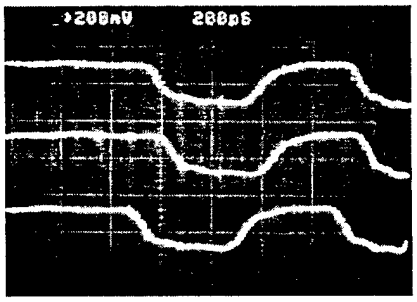
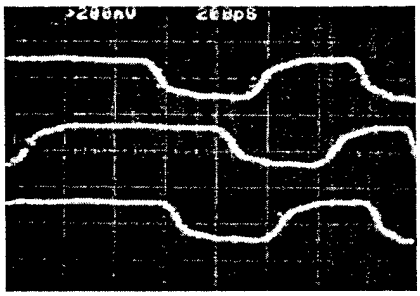


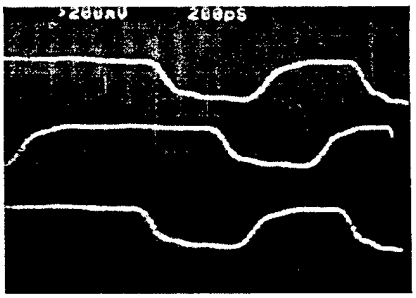
Fig. 19. Coarse Delays Adjustment



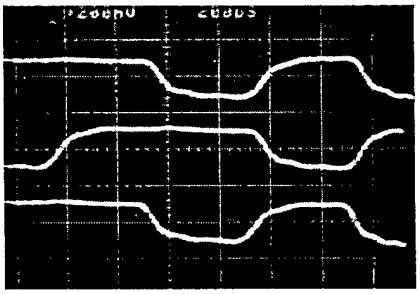
(a) Delay Resolution: 100 ps



(b) Delay Resolution: 200 ps



(c) Delay Resolution: 300 ps



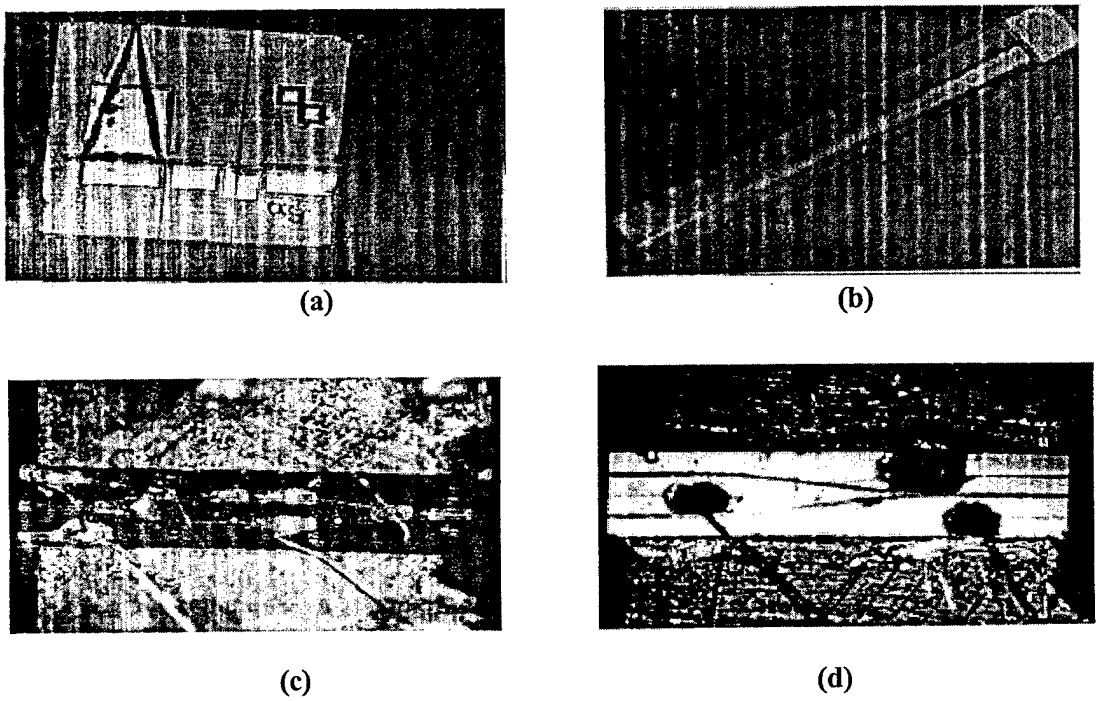
(d) Delay Resolution: 400 ps

Fig. 20. Fine Delay Adjustments

Since the most difficult in aligning the phase is the last few stages, we also demonstrate the phase alignment of the last three stages to prove the function of the cell synchronization unit. A reference clock is distributed in the whole switch system and used by all inputs as a common alignment basis. The electronic part of the unit has correctly operates at 2.5 Gb/s and is being integrated with optical devices for complete testing. The generated optical delays as small as 100 ps were achieved. Fig. 20 (a), (b), (c), and (d) show the delays generated from 100 ps to 400 ps. The accuracy can be as small as an ¼ bit at 2.5 Gb/s.

8. Wavelength Converters :

We can use the cross-gain and the cross-phase modulation effects in SOAs to do wavelength conversions. From our recently discovered "gain decompression effect" [Paper #3] we found that we can use either the side injection [Conf #1,2] or the long SOA cavity length [Paper #3] to achieve high-speed wavelength conversions. We have made devices for implementing either schemes into our conversion devices and found that the later is more effective. Fig. 20 shows pictures of different types of ? converters: two different side-injection converters, an all-active Mach-Zender converter with separated injection branches and an all-active Y interferometer. Conversion results at 5 Gb/s (the speed limit of our BER testing set) are easily achieved as shown in Fig. 20. The input 0-1 stream is complementarily converted to the output stream. The scale is 500 ps per division.



(a) (b)

(c) (d)

Fig. 21 Wavelength Converters with Different Structures
(a) (b) Side-injection, (c) Mach-Zender (d) Y-interferometer

Besides using the cross-phase modulation effect to do wavelength conversions, we can use the cross-gain modulation effect to achieve wavelength conversions. **We have proposed and demonstrated a new effect, the gain decompression effect**, to explain how an ultra-high speed conversion or logic operation can be achieved [paper #3]. The effect relies on the intra-band carrier relaxation time and the operation speed of devices is limited around 100 femto-second ranges. We also have proved that to achieve very high-speed wavelength conversions or all optical logic operations, a long SOA device with a very high bias current is needed. Unfortunately, such an operation put a very high requirement on the quality of the

antireflection (AR) coating at the device facets. A long SOA (> 1000 ?m) with a normally available AR coating at ~ 1% reflectivity can easily reach lasing situation at a bias below 100 mA. The gain of the device will thus be clamped at the threshold and the device will perform poorly on speed.

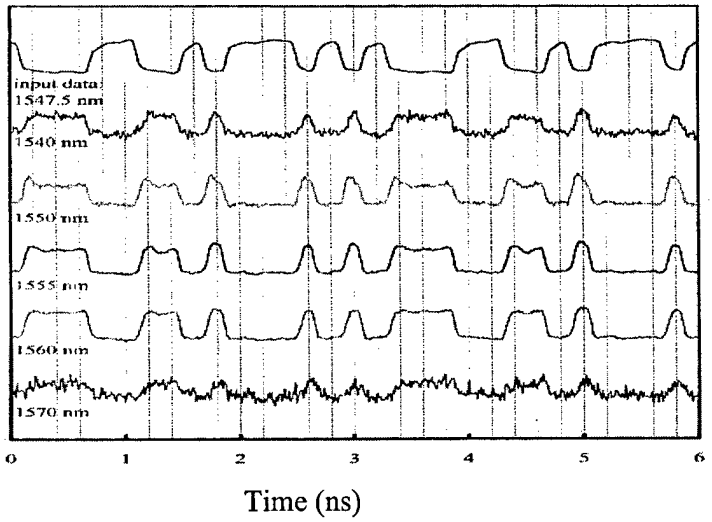


Fig. 22 Wavelength Conversion to Different Wavelengths at 5 Gb/s

To obtain very fast all optical switching and logic operations, we designed and fabricated two-section SOAs. By adjusting the injected carrier density of one of the two sections (shorter one) below its transparency carrier density, we can keep the device from lasing even when the long section is biased very high. The strict requirement of very low reflectivity AR coating is relieved with this device.

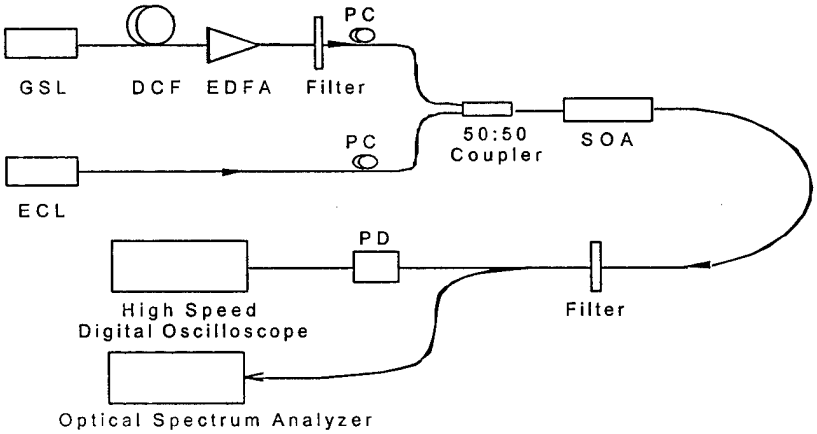


Fig. 23. The experimental setup of gain recovery measurement

The device we made is a two-section (500 ?m and 1500 ?m long, respectively) multi-quantum well (MQW) SOA with a gain peak around 1.55 ?m. To demonstrate all optical logic operation, we have used the device as a NOR gate. Three lights are injected into the SOA, where the long section is biased at 170 mA. Light A and B are used as the logic input. The input power of light C is kept constant (cw), and its output can be expressed as $\overline{A ? B}$. Limited by the speed of bit-error-rate test set, the NOR gate is operated at 5Gb/s.

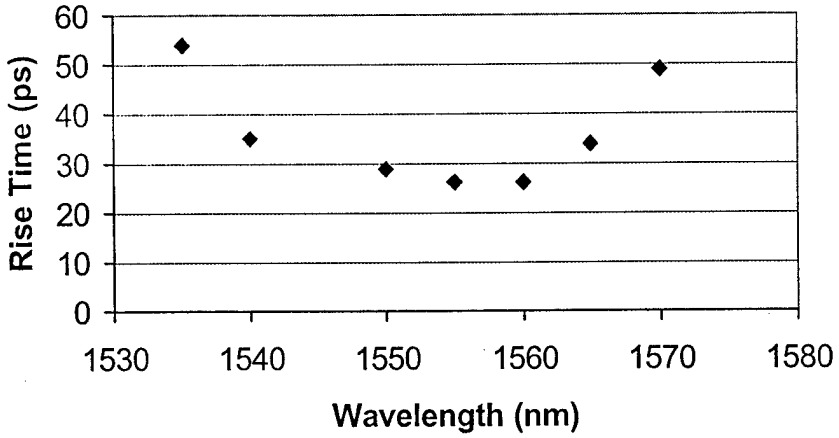


Fig. 24 (a) Wavelength dependence of rise time

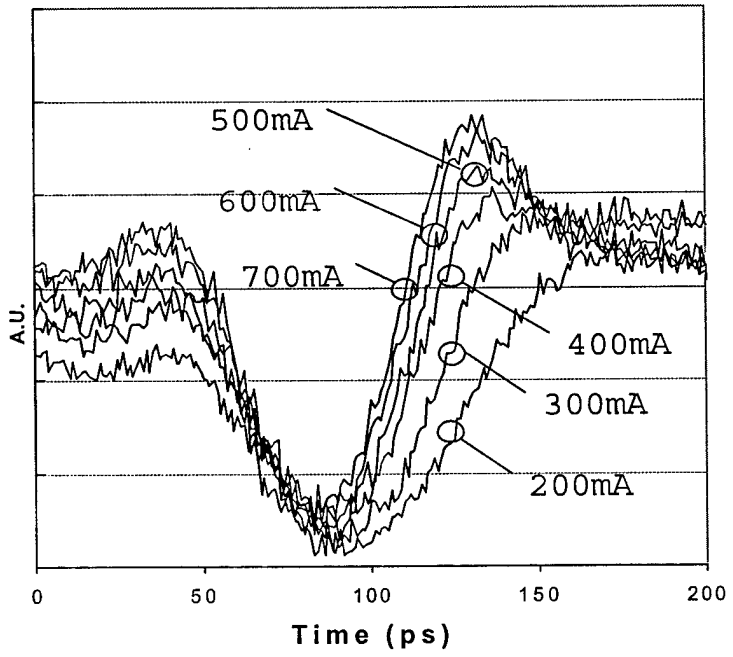


Fig. 24(b) Probe output waveforms at different bias current

In order to study the speed of our device and to optimize the operation parameters, we have measured the gain recovery time using the probe-pump scheme at different probe wavelengths and injection current. The setup is shown in Fig. 23. We used a gain switched DFB laser (GSL) as the pumping source (wavelength 1547nm). After the compression of a dispersion compensation fiber (DCF), the amplification of an EDFA, and the filtering of a FP Filter (1.3nm bandwidth), a pumping pulse of 30ps with a peak power near 1W is obtained. The probe source is an external cavity tunable laser (ECL) with a tuning range from 1530nm-1570nm. After the SOA and a FP filter (Bandwidth 0.6nm), the probe output is sent to a 40GHz high speed photodetector (PD) and displayed with a 60 GHz digital oscilloscope.

Fig. 24(a) shows the SOA bias current dependence of the recovery time. The probe wavelength is fixed at 1550nm and ECL output power is at 5.5 dBm. The gain recovery time changes from 45ps to 13ps corresponding to bias current from 200mA to 700mA. Afterwards the speed is limited by the resolution of our measurement setup. Fig. 24(b) shows the probe wavelength dependence of gain recovery time at a constant injection current (I = 600mA). The ECL output power is kept at 3dBm when operated at different wavelength. With constant input powers for both the pump and probe, the gain recovered fastest at the device gain peak and slower at the higher and lower wavelengths. This again shows that to be able to increase the SOA gain is essential to obtain very high speed all optical operations.

6. WDM Memories:

We have demonstrated a scalable and modularized random access fiber loop memory for application to optical packet-switched networks. The experimental setup of a random access fiber loop memory is shown in Figure 25. Directly modulated distributed feedback (DFB) lasers are used as multi-wavelength sources to generate the packet at different wavelengths for the experiment. An 8-wavelength (1549.3 nm to 1560.5 nm) waveguide-grating-router (WGR) with 200 GHz channel spacing is used as wavelength demultiplexer in the fiber loop. A 1x2 optical space switch (SW_i), which is currently composed of two $LiNbO_3$ modulators and controlled by two complementary signals, is used to switch packets in and out of the loop, one per wavelength. The switches are replaced by an array of integrated 1x2 semiconductor optical amplifier switches fabricated in our laboratory. An erbium doped fiber amplifier (EDFA) is employed in the loop to compensate the loss.

In order to scale up, for example, to a 128-packet memory size (packet loss rate is below 10^{-8} for output buffered packet switches), the two Nx1 fiber combiners would need to be replaced by WGRs in order to reduce splitting/combining loss. Unlike other proposed systems, our system does not require any fast tuning filters. Moreover, all the components in our system can be modularized or integrated. The "gain-clamping loop" is designed to provide long-term reliability of the optical loop memory and is explained in the next section.

Figure 26 shows the packet outputs at the monitoring port and after the switches at different wavelengths and different delay times (randomly chosen). A tunable filter is used at the monitor port to monitor the stored packets at different wavelengths. Each packet has 127 packet bits (2^7-1 PRBS). In the figure, the wavelengths of the two packets are 1549.3 nm and 1550.9 nm,

respectively. The waveforms of the first 15 and 24 turns of the two packets can be observed at the monitor port. After they are switched out through the switch port, they are removed from fiber loop and no residue is observed afterwards. A blow-up of the waveforms in Figure 26 for the original packet and the packet after 25 circulations is shown in Figure 27. The small difference between the two packet waveforms is likely to be caused by EDFA's Amplifier Spontaneous Emission (ASE) noise.

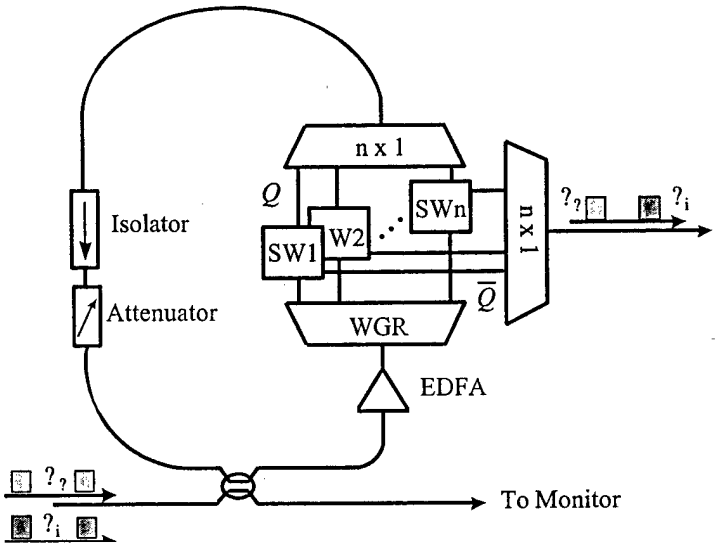


Fig. 25 WDM Fiber Loop Memeory

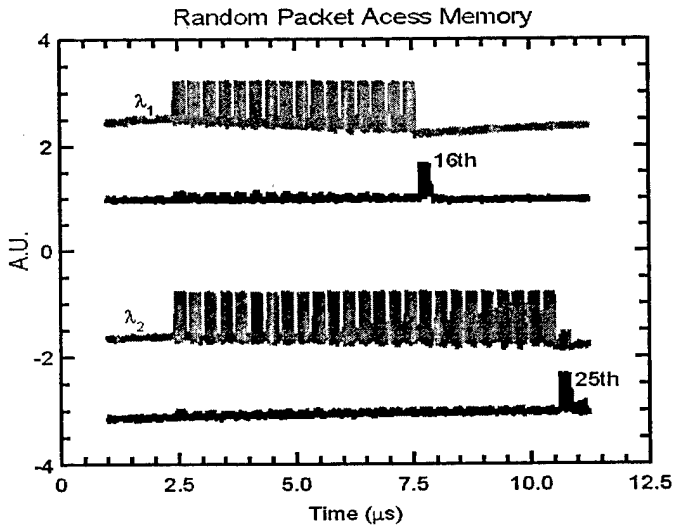


Fig. 26 Output Packets Waveforms.

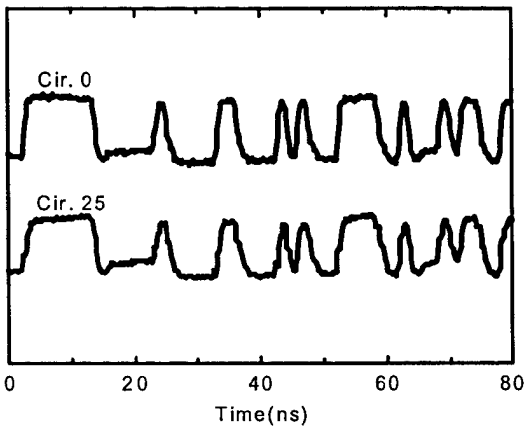


Fig. 27 WDM Memory Output Waveforms Before and After the Memory Operation

6.2 Stabilization of multichannel fiber loop memory by gain clamped optical amplifier.

Optical buffer memories are essential components in an all-optical packet- or cell-switched network to resolve contentions. However, during the memory operation, signal levels inside the loop can fluctuate when there are packets or cells dynamically written into or read out of the memory. This can seriously affect the stability of our memory as well as backbone switch operations. The fluctuation is primarily due to an accumulated effect of the unclamped EDFA gain in a loop. Although there is only one EDFA, optical signals pass through the EDFA many times before they are read out of the memory. That is similar to a WDM system with a chain of cascaded EDFAs. However, the response time of the system is much faster due to the much shorter fiber used in the memory loop (<60 m in our case). Since the EDFA is nearly homogeneously broadened, gain clamping, using internal laser oscillation, can be utilized to obtain stabilized operation. In this section, we present our experimental results of using a gain-clamped EDFA to stabilize gain and signals in a WDM loop memory. Our results show that signal fluctuation can be significantly reduced and stabilized memory operations can be achieved. The experiment setup of the WDM optical fiber loop memory with a gain clamped EDFA is shown in Figure 28. The experiment was performed with optical packet of 512 bits at 2.5Gb/s. The fiber loop is a little longer than the packet length to provide guard time for the packet. This system is designed to simulate an 8-channel system. In this experiment, the optical signal at 1554nm is used as the signal channel (ch. #1), optical signal at wavelength 1550nm is used to simulate the 7 other channels (ch. #2-8) by setting its power to a corresponding level. Two tunable optical bandpass filters are used in the loop as demultiplexers and noise filters for the signals. Two 2x2 optical space switches (SW1, SW2) are used to control the loop memory's operation. An EDFA is used to compensate the loop loss caused by optical couplers, optical filters and optical switches. A tunable attenuator is used in the loop to keep the loop's net gain to be unity at beginning.

To realize gain clamping, an optical loop with a tunable optical bandpass filter is introduced to the WDM fiber loop memory. By tuning the wavelength of the optical filter, the gain clamping

condition can be controlled through the wavelength dependent slope of the EDFA's gain profile. The clamping level (determined by the loss of the clamping loop) and wavelength should be carefully selected to obtain signal stabilization operations and provide a large enough loop (the packet circulating loop) gain at the same time. In our experiment, the clamping loop was set to have a total loss of about 13dB. The clamping wavelength is selected between 1557nm and 1565nm to ensure a strong gain clamping effect and leave enough optical bandwidth for WDM applications. Figure 29 shows the optical spectra of data signals and the clamping signal.

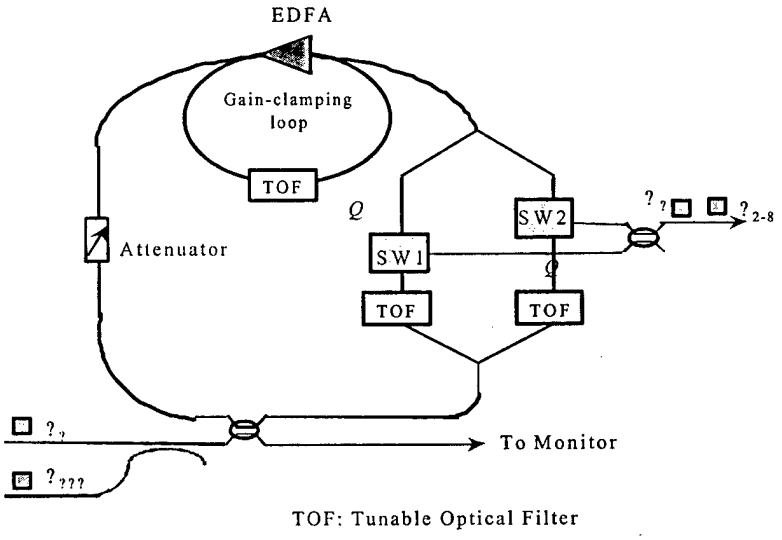


Fig. 28 Gain-clamped WDM Memory

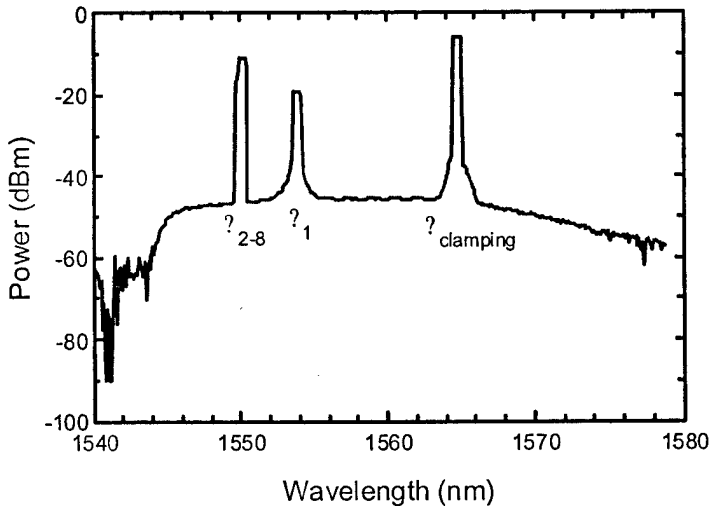


Figure 29 The Optical Spectra of Data Signals and The Clamping Signal.

The input power of ch. 1 is –20 dBm. It is stored in the loop memory and circulates for 15 times before being taken out. The add/drop channel (ch.2-8) is set to -? , -20, -15.2 and -I 1.5dBm to simulate the case of 1 channel, 2 channels, 4 channels and 8 channels in the loop, respectively. From Figure 30 (a) we can see that the signal level vanes a lot when the EDFA is not gain clamped. The signal even vanished when only 3 channels were added to the loop. As shown in Figure 30(b), when the EDFA is gain clamped by the clamping loop with a tunable optical filter, the signal fluctuation is greatly reduced.

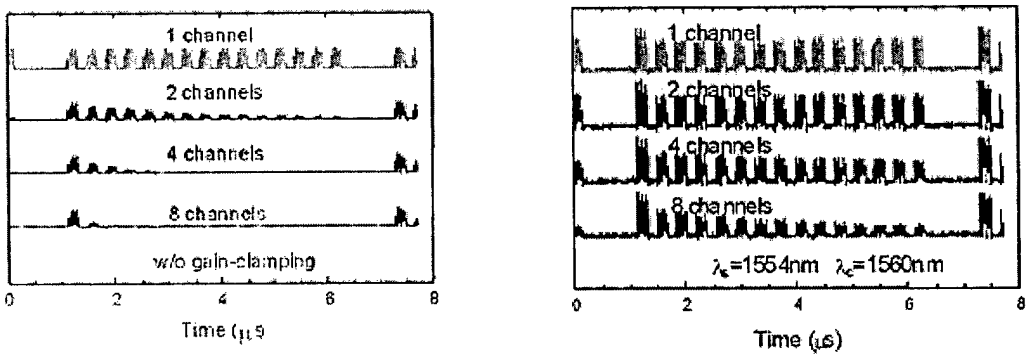


Fig. 30 (a) Without (b) With Gain Clamping

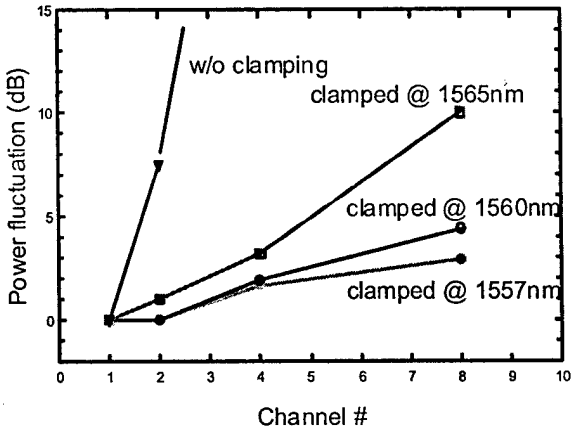


Fig. 31 Power Fluctuation as a Function of Wavelength and Channel Number

We measured the signal power fluctuations caused by adding 1-7 channels in the case of no gain clamping and with gain clamping at wavelengths of 1565nm, 1560nm, and 1557nm, respectively. The result is shown in Figure 31. If there is no gain clamping for the EDFA, the signal power fluctuation in the loop is more than 10 dB with the addition of only 3 channels. When the gain clamping loop is turned on, the signal power fluctuation is greatly reduced. However, even in the gain clamped case, the stabilization condition is strongly dependent on the clamping wavelength. The maximum fluctuation is 10 dB, 4.4dB and 2.9dB for clamping wavelengths at 1565nm, 1560nm and 1557nm, respectively. It can be explained from the EDFA's gain profile that the gain-clamping wavelength will experience different gain at different wavelength. To operate at

shorter wavelengths can provide stronger gain clamping effects than to operate at the longer wavelength side of EDFA. In conclusion, we have experimentally studied the gain-clamping effect of an EDFA in a WDM fiber loop memory. Less than 3dB signal fluctuation during packet read/write can be obtained when the gain clamping is employed.

6.3 All Optical Dynamic Random Access Memories (DRAMs)

The small amount of ASE noise accumulation can degrade the signal stored in the loop memory and can lead to reliability problems. To solve the problem, a dynamically refreshed optical loop memory was proposed and demonstrated [Conf. 24]. The proposed dynamically refreshable WDM optical loop memory is shown in Fig. 32. The fiber loop is a little longer than the packet length in order to provide a guard band of approximately 20% with respect to the loop round trip time. A set of n 1x2 optical space switches (SWL1-SWLn) is used to selectively remove a packet from the loop for purposes of refreshing or forwarding to the next stage of the optical network. In the former case, the packets are periodically extracted from the loop memory and refreshed in the refreshing unit which consists of an optical/electrical (O/E) converter, a regeneration circuit, and an E/O converter. The refreshed packet is then reintroduced into the loop memory at its original wavelength through a tunable wavelength converter. Precise control of the optical delay, ?, is required in the refreshing unit to ensure that the in-loop packet is completely removed before the refreshed packet re-enters to the loop. The electronic control unit arbitrates the selection of wavelength for new packets in order to prevent conflicts with existing or refreshed packets. Since the packets require only periodic refreshing, a single refreshing unit can be multiplexed to satisfy the refresh requirements for each of the packets in the WDM loop memory.

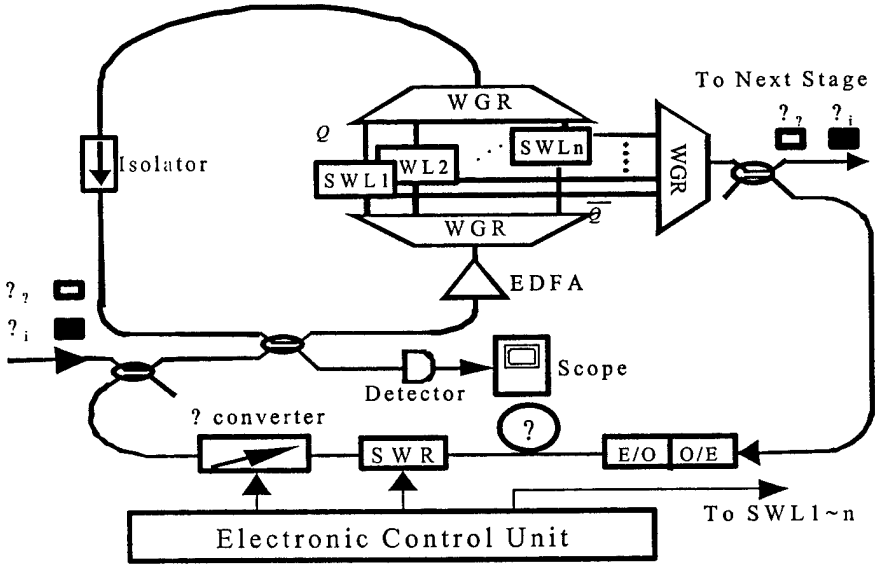


Fig. 32 Refreshable DRAM

Fig. 33 shows the waveforms from a refreshing experiment for a packet optically encoded at a wavelength of 1552.5 nm. The optical signal is monitored after the 3dB coupler where packets are fed into the loop and again after the 1x2 optical space switch. The experiment was performed

at a frequency of 622Mb/s using a packet size of 128 bits. An 8-wavelength (1549.3 nm to 1560.5 nm) waveguide-grating-router with 200 GHz channel spacing is used as wavelength demultiplexer in the fiber loop. Fig. 33(a) shows the electronic control signals, in which the upper signal is used to disable the refresh unit when a new packet is being sent into the loop. The lower signal is used to control the optical switches inside the loop for the packet refreshing operation. The upper waveform of Fig. 33(b) is the new packet from the optical sources. The optical packet, after four cycles through the loop without refresh, is shown as the middle waveform while the packet with refresh is shown along the bottom. In this experiment, the packet is refreshed after five cycles through the loop. Due to the limitations of our current control electronics, each packet is only refreshed three times before a new cycle is started. It should be noted that in a working system, the refresh rate would be determined by the S/N ratio of the EDSA. Therefore, the proposed OLM with refresh can be used to build a system that provides permanent optical packet storage, which can operate at very high frequencies.

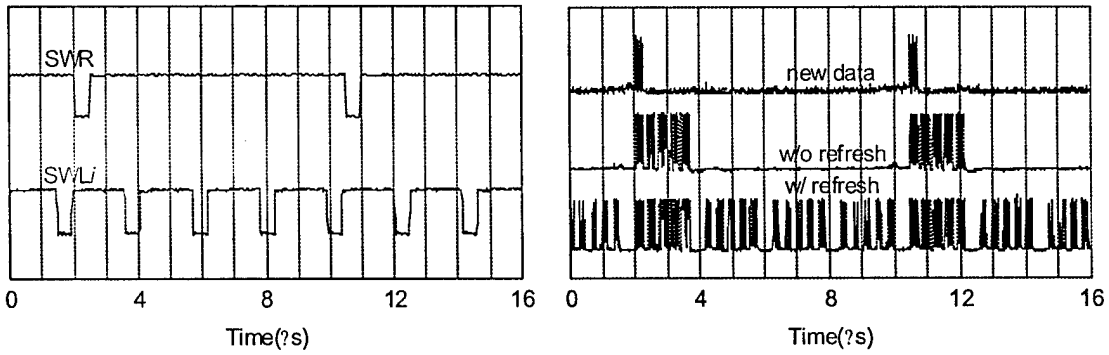


Fig. 33 Results of refreshable DRAM (a) Electronic control signals (b) Optical signals

7. Cell Concentrators Using Fast Tunable Active Filters :

Fast tunable filters are used in our work to select packets for output. We have tested our fabricated tunable active filters and used them as wavelength demultiplexers in an 8-wavelength system. It has insertion gain instead insertion loss. The DBR filter is composed of gain, phase, grating, and post-filter gain sections. Error signals for wavelength control and dynamic gain control are extracted from the gain section and feedback to the grating section and the gain section, respectively. The post-filter gain section can be used to switch the output on or off. The central wavelength of the DBR filter can be easily tuned and locked to a desired channel by changing the grating bias current.

Active optical filters have the advantage of providing insertion gain instead of loss and are potentially good candidates for WDM demultiplexing. With its capability of tuning, locking, and gain control, the active filter is also possible to eliminate the problem of the band-narrowing effect caused by cascading mis-aligned passive optical (de)multiplexer in all-optical networks. We have studied the performance of DBR active filters used as demultiplexers in very dense WDM system. Penalty-free transmission was achieved with channel spacing of 25GHz at 2.5Gb/s.

The system setup is shown in Fig. 34. A 1.53? m DBR laser and a tunable external cavity laser (ECL) are externally modulated by a $LiNbO_3$ modulator at 2.488Gb/s with 2^{31}-1 PRBS (pseudo random binary sequence). The modulated signals are coupled into one 1.53? m DBR four-section active filter. The ECL can be continuously tuned to provide the signal source as a crosstalk channel when the DBR laser is used as the signal channel. The tunable active filter we used is an integrated four-section InGaAs/InGaAsP distributed-Bragg-reflector (DBR) laser amplifier, which is composed of a gain, a phase, and a grating section followed by another gain section. With a carefully designed cavity length and a well-controlled grating-coupling coefficient, the active filter allows only one single below-threshold Fabry-Perot (FP) mode in its cavity. Using the ECL, we have measured the DBR filter passband at different input power levels. The passband is given in Fig. 35(a) for an input power of –20 dBm with active filter biased at 0.98 I_{th}. Due to the gain saturation and the non-linear pulling effects, the filter peak wavelength shifted to longer wavelengths. Net fiber-to-fiber gain is always obtained for input power between –30 dBm and –15 dBm.

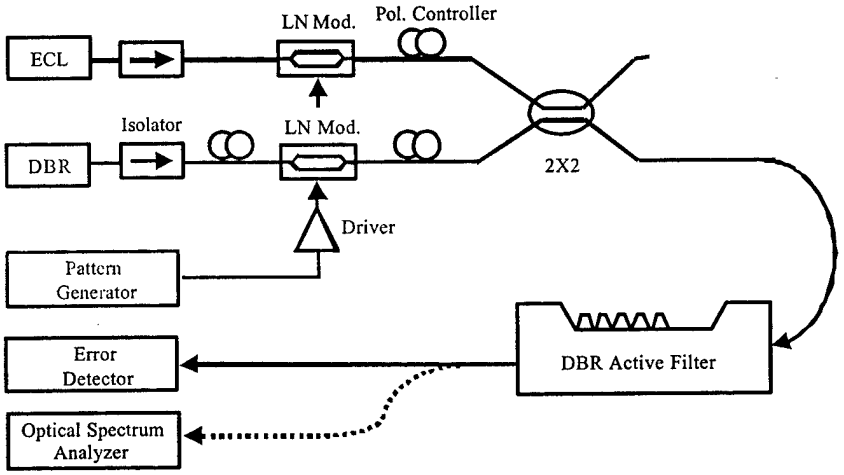


Fig. 34 System Setup for Crosstalk Measurement of DBR Active Filters

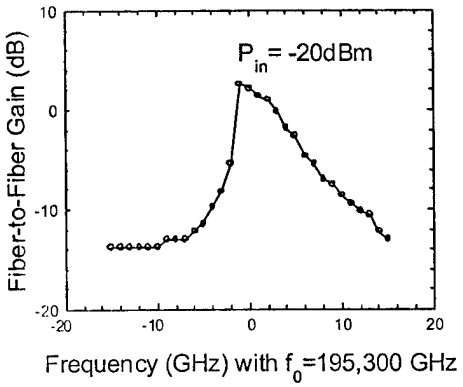


Fig. 35(a)

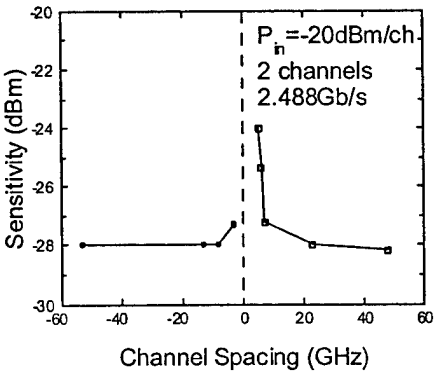


Fig. 35(b)

Fig. 35 (a) Passband of a DBR Active Filter (b) Receiver Sensitivity measured for different channel spacing @ BER=1? 10^{-8}

In the system measurement, we first align the signal channel with respect to the filter's central frequency to obtain the optimized receiving sensitivity. We then tune the ECL to sweep across the signal channel wavelength to observe the receiving sensitivity degradation. In the study, both channels have an input power of –20 dBm and the filter is biased at $I=0.98I_{th}$. The receiving sensitivity is measured for different channel spacing. The result is shown in Fig. 35 (b) and there is no power penalty for the system with a channel spacing larger than 20 GHz at either the longer or the shorter wavelength sides. The crosstalk induced power penalty becomes very serious when the channel spacing is less than 10 GHz at the longer wavelength side and is less than 15 GHz at the shorter wavelength side, respectively. This power penalty asymmetry shows that channel, which are sitting at the long wavelength side of the active filter is more stable.

An 8-channel WDM system with 0.8nm (100GHz) spacing was demonstrated using such filters as shown in Fig. 36. A channel rejection ratio of 20 dB was achieved when the average input power of each channel was at -30dBm. The extinction ratio reduced to 15dB when the signal level was increased to -25dBm/channel, due to the gain saturation of the active filter. The saturation power of the device will be improved by using a ridge type waveguides.

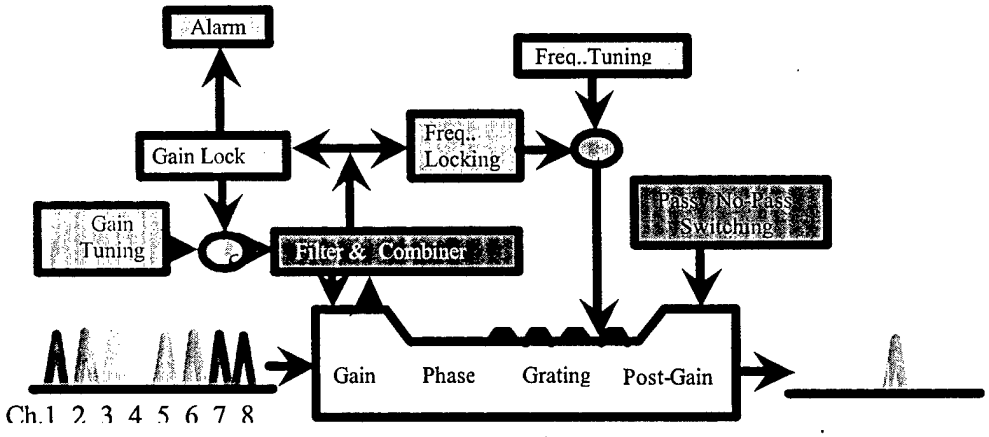
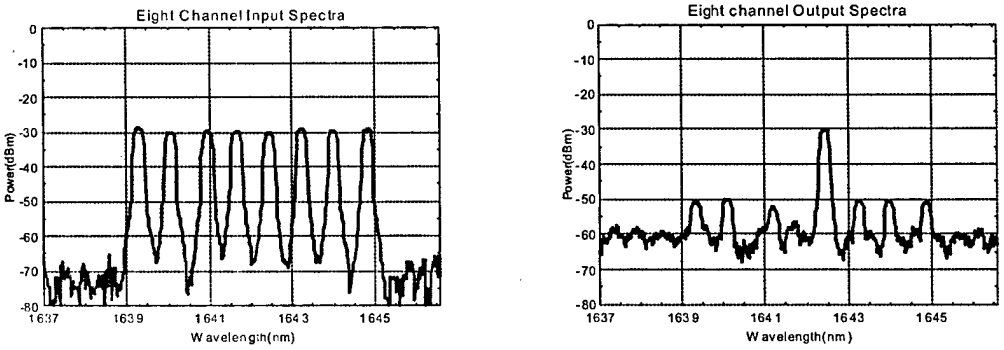


Fig. 36 (a) Single Channel Setup



Lossless filter, 20 dB rejection ratio @ Pin=-30 dBm, 15 dB reiection ratio @ P_{in}= -25 dBm

Fig. 36 (b) Channal Selection in the 8-channel System

8. Route Controllers :

The route controller implements routing, contention resolution and multicast by means of decision logic and queues. An idle wavelength queue is used for wavelength assignments. Counters are used to set in-loop time duration of each cell with a particular wavelength. Finally, when an output port does not have any cell to send, the FPGA circuit sends an idle cell by sending the cell that is supposed to be output from the other output port. The route controller operates at the cell time which is 4MHz while the bit rate is 2Gb/s. The input/output relationship of the Route Controller is shown in Figure 37.

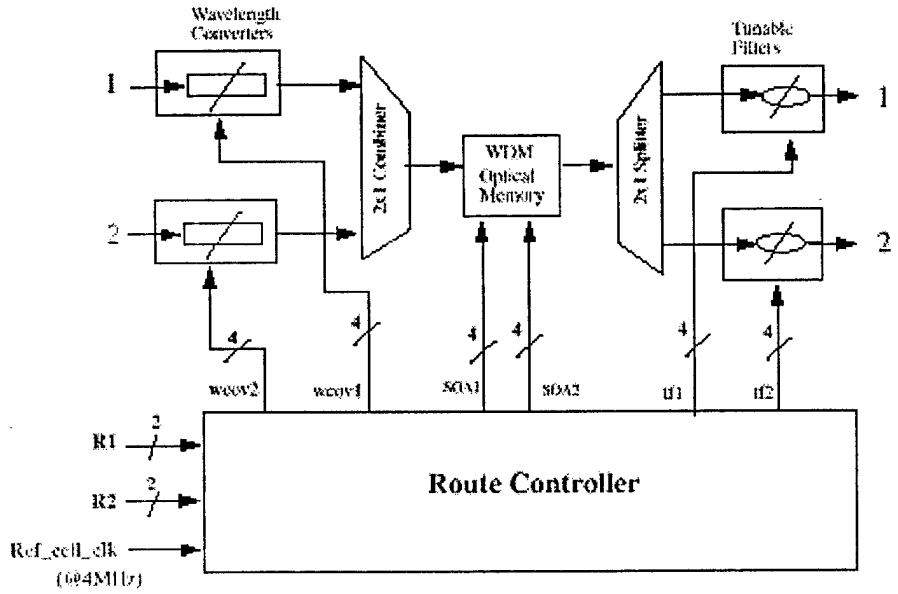


Fig. 37. A Top-Level View of the Route Controller Circuits

All the functions of the route controller except clock, power and driver circuits, are implemented by an FPGA chip. These functions include keeping track of cells in the optical loop memory, performing wavelength reservation and route control. The functions programmed into the FPGA are implemented by a VHDL program whose text length is 450 lines (Appendix I). The program downloaded to the FPGA is prepared on the Xilinx Foundation 3.1i development system.

The VHDL style of programming and the FPGA allow testing of different ideas and their implementation fast. For example, a simple VHDL code is written to specifically test the loop memory by using the same hardware. The code generates loop memory control signals to keep a cell in the loop memory for a particular duration, for example 14 cell times.

The final Route Controller circuit is built in a custom Printed Circuit Board (PCB). Before the custom PCB was built, a similar circuit was built on a protoboard. The 10"x 18" protoboard

contains a 3.8"x 3.6" APS-X240 development PCB with a Xilinx Virtex XCV800 chip, dip switches to adjust the delay of control outputs, driver chips for interfacing to the analog circuits and SMA connectors for direct connect to the analog circuits.

The custom PCB is a 6"x 9" 6-layer PCB containing a XCV300 FPGA chip, clock, power and driver chips as well as dip switches and SMA connectors. Appendix II Fig. 1, 2, 3 show the FPGA, clock and power subcircuits of the custom Route Controller PCB, respectively. The main advantage of the PCB is improved signal quality by placing wirings on the board, rather than by "fly wires." The FPGA chip is changed from the XCV800 type to the XCV300 since the protobard experiment showed a smaller one would be sufficient. The board layout is prepared by using the Protel 99SE development platform.

The connection of route controller outputs to the loop memory is done on commercial switches, not SOA switches. These commercial switches perform the same function as the SOA swithces and are used due to device constraints at the time. The input to the switches is digital. The wavelength converters on the other hand are implemented by a set of four lasers. Each laser generates light at a specific wavelength and requires an analog signal with a different dc offset and pulse amplitude. Therefore, digital wavelength coverter outputs of the FPGA have to be connected to a series of four opamp circuits, one for each wavelength. Each opamp circuit is identical and allows the dc offset and pulse amplitude to be adjusted by using potentiometers.

The custom PCB has two sets of dip-switche to adjust the delay of any one of the 24 outputs. This is in contrast to the protoboard circuit, which contained 24 sets of dip switches. The first dip switch as seen in Figure 3 selects a control output. The second one inputs the amount of delay in increments of 8 ns. The longest delay is 120 ns which is longer than one half of the cell time.

8.1 2x2 Switch Experiments

We have demonstrated a 2x2 WDM ATM Multicast Switch using the devices and circuit boards we built in the program. The detailed results are shown in the following.

Fig. 38 shows the overall setup. Fig. 39 shows all the electronic control circuit boards. Fig. 40 shows the VCI overwriting units. Fig. 41 shows the optical setup. Fig. 42 shows the FPGA route controlling setup and the optical loop memory.

When the optical packets are sent into the two input ports, we use repeated patterns so that we can see them clearly in the oscilloscope. Fig. 43 shows the input packets. After the VCI overwriting units their older headers are replaced with newer headers but the packets are still transmitted with the older payloads. This is shown in Fig. 44-48. Before send them into the optical memory for contention resolution and route controlling they have to be aligned in the time domain using the synchronization circuits. The synchronization signals including cell clocks, byte clocks and bit clocks are generated from the cell delineation units and send to the synchronization circuit board to control variable optical delays. The same synchronization signals

are used to sync. the route control signals and switch packets in and out the memory as shown in Fig. 49 and 50.

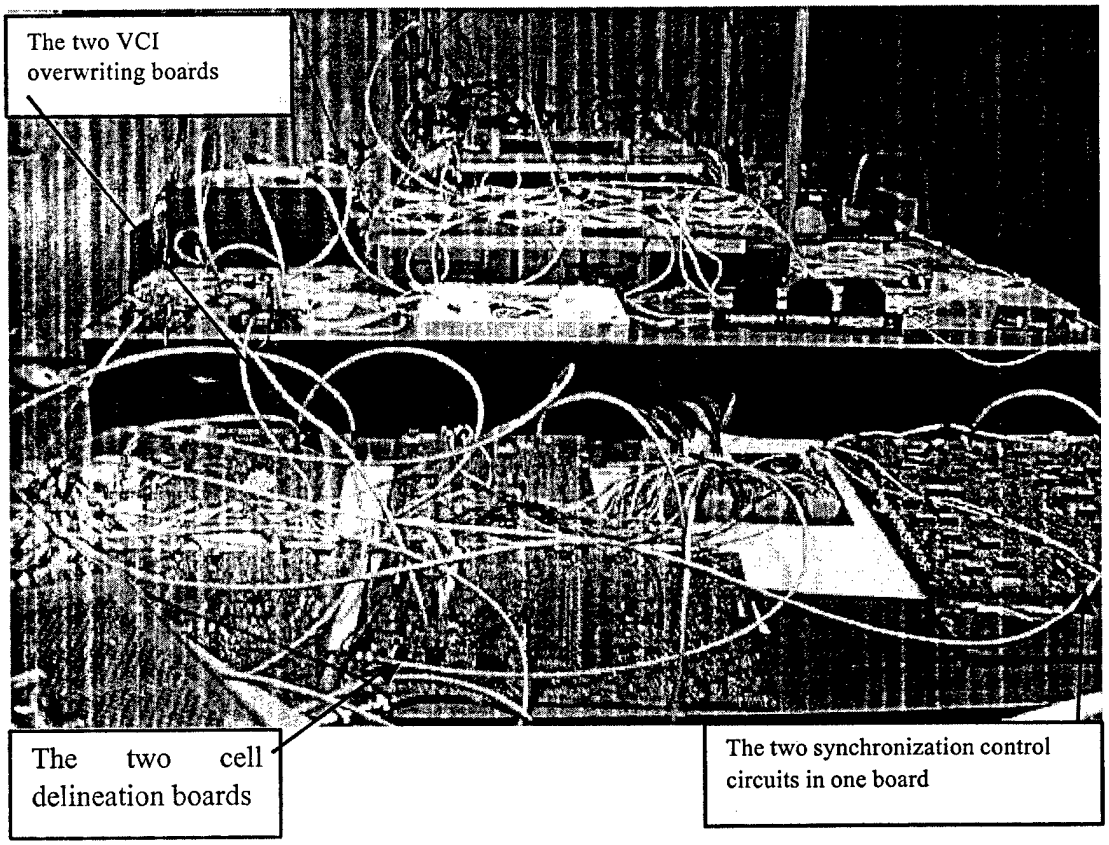


Fig. 39 Experimental setup

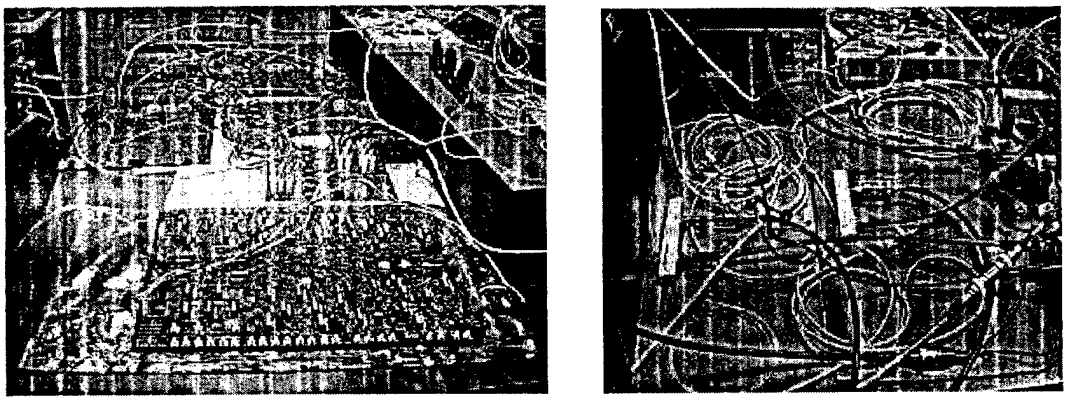


Fig. 40 Electronic control circuit boards and VCI overwriting units

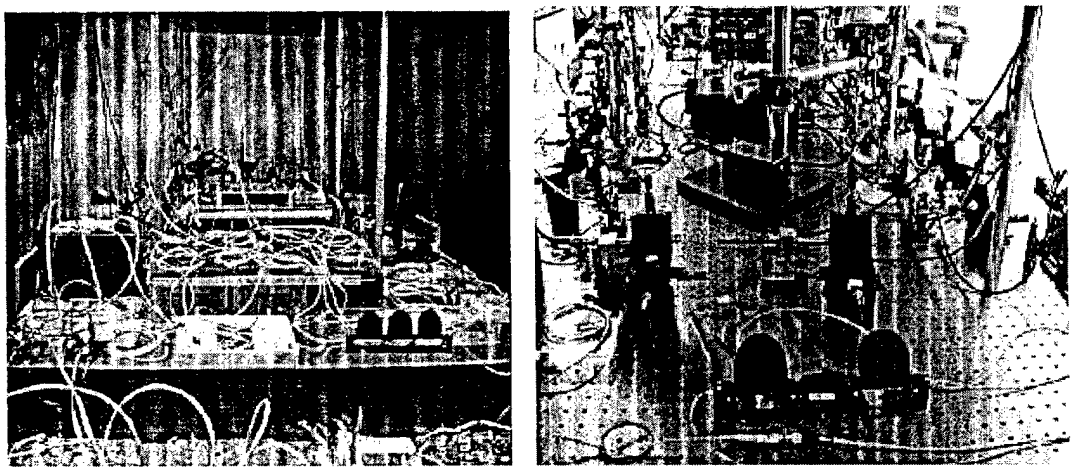


Fig. 41 Optical set up

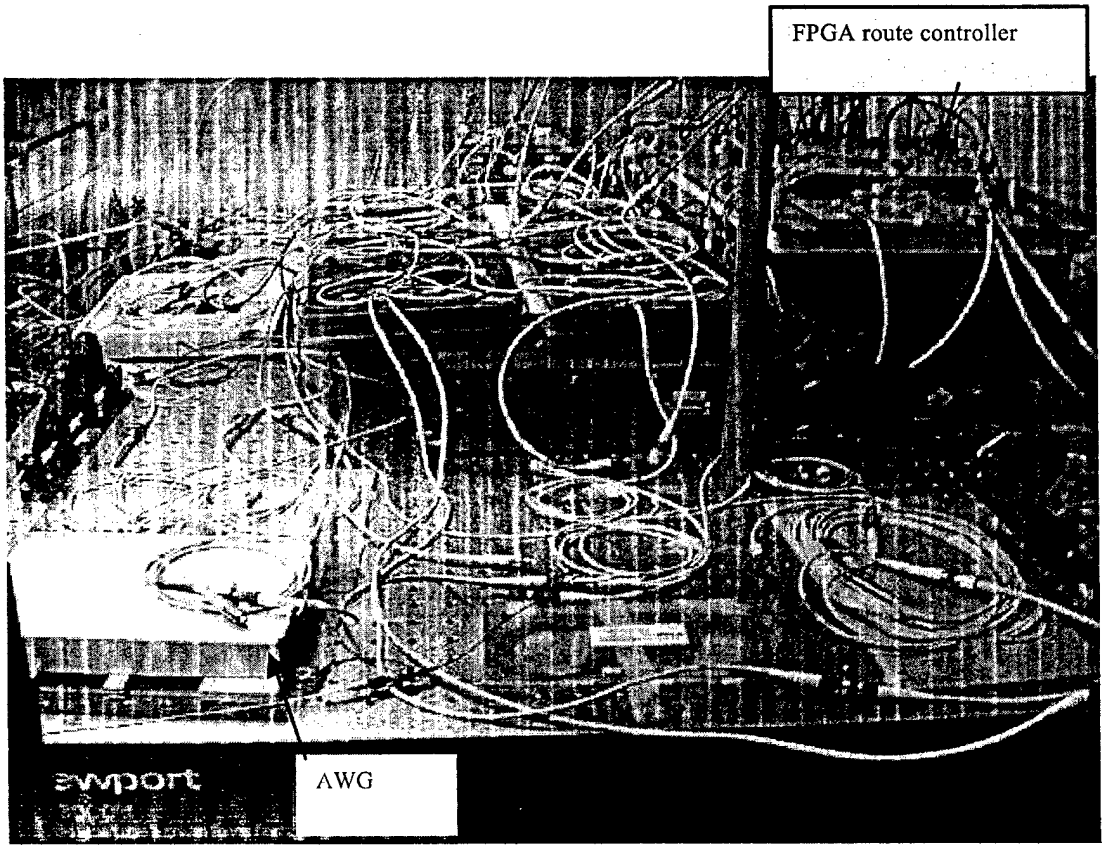


Fig. 42 Route controlling and the loop memory

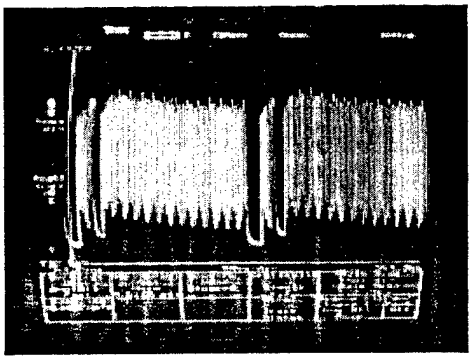


Fig. 43 Two input packets

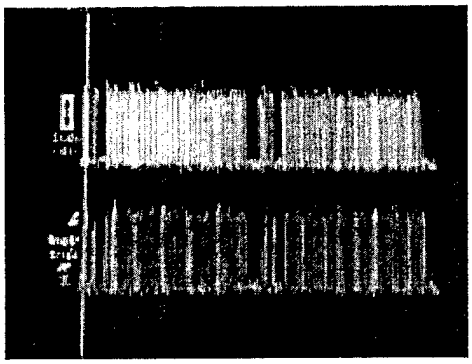


Fig. 44 The old and new packets (header swapped)

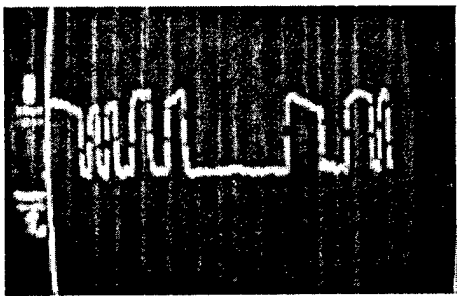


Fig. 45 (a) Older header and (b) New header

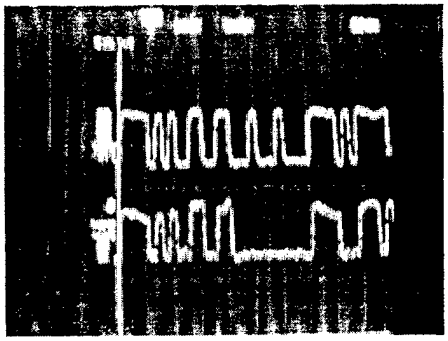


Fig. 46 Two headers synchronized

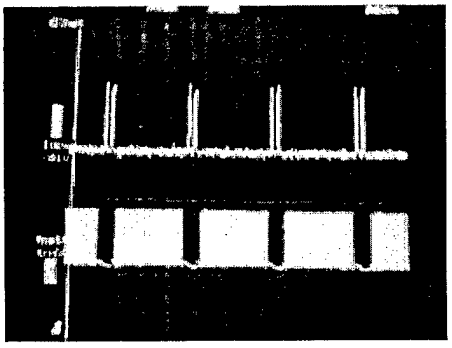


Fig. 47 New header and old payload

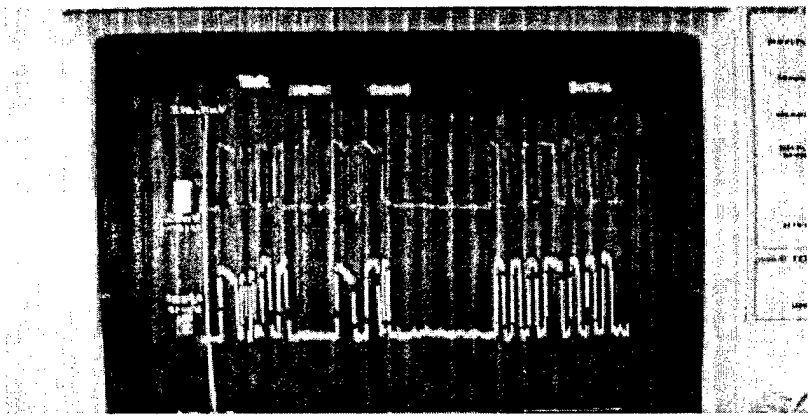


Fig. 48 The old header is replaced with the new one

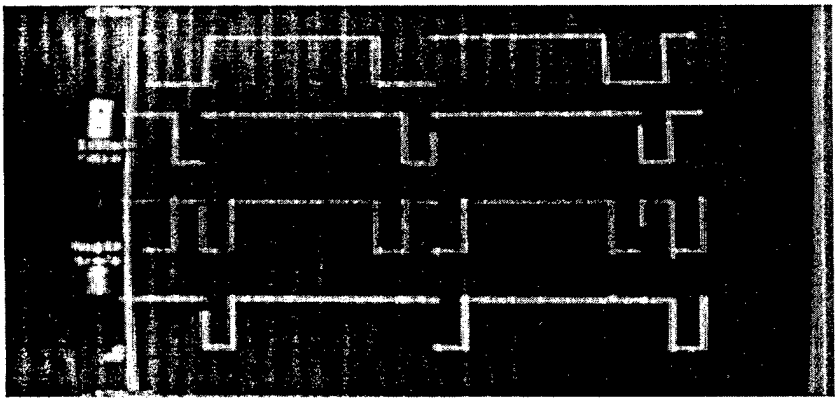


Fig. 49 Switching control signals

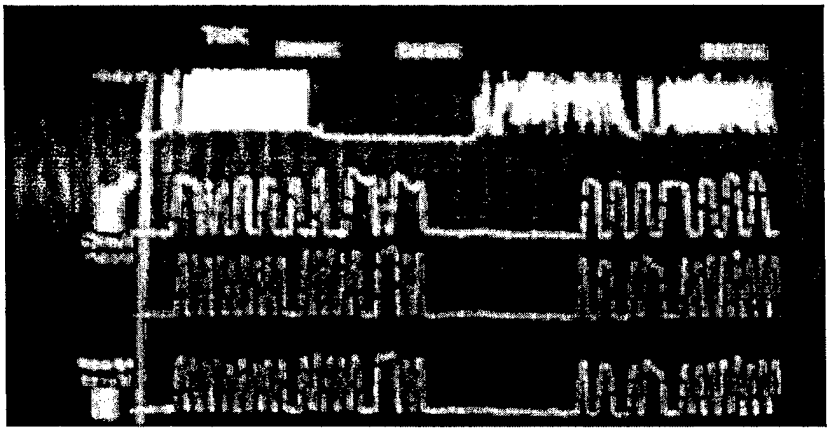


Fig. 50 Wavelength3 and wavelength4 (wavelength4 switched out after one round in the loop)

9. Broadband Optoelectronic Devices to Improve Scalability:

After the switch system demonstration, our works are focused on the scalability of every part of the switch system. Our goals are: 1. Increase the capacity of the all-optical memory one hundred times. 2. Increase the wavelength conversion and the optical space switch wavelength coverage range accordingly. 3. Increase the broadcast-and-select switch size one hundred times. The key to achieve all above goals is to build a new type of material/device that can have extremely broad wavelength tuning range. Two types of gain materials will be studied in this research work: a. The Esaki-junction type and b. The selective-area-growth (SAG) type of gain materials.

a. The Esaki junction type of gain materials: Fig. 51 (a) shows the structure of the Esaki type of gain material. The Esaki-junction type of gain material is composed of N multi-quantum-well (MQW) p-i-n regions each with a different wavelength peak. In between any two of the N MQW p-i-n regions, there is an Esaki junction. An electron will start from the very end n side, pass through each MQW p-i-n region, tunnel through each Esaki junction, and finally reach the very end p side. One electron will generate N photons, each with different wavelengths. Broadband gain material can thus be achieved. The advantage of using this type of material is that one electron can pump multiple photons and the quantum efficiency is higher. Compared with using the asymmetrical MQWs in one p-i-n region, the Esaki-junction type of gain material can allow dramatically different MQWs to be set in different regions without worrying about balancing carrier collection efficiency at different wells. Fig. 51 (b) shows the results of a 2-band Esaki-Junction laser we made recently in our laboratory. The peak wavelengths of the two gain materials are at 1450 and 1550 nm. Although the gain profile is not yet smooth in this case, they can be independently adjusted to reach a high-gain, broad-tuning-range, high-slop-efficiency semiconductor laser material.

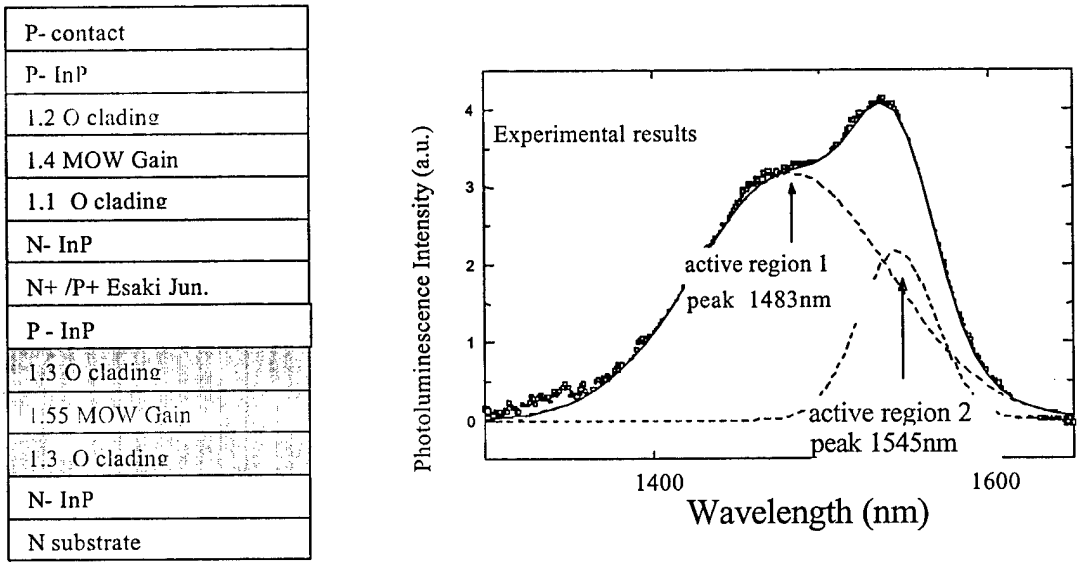


Fig. 51 (a) Layer structure of an Esaki Junction material with two different gain media (b) Measured photoluminescence of the grown material with two gain peaks.

b. The Selective-Area-Growth (SAG) type of Gain Materials: The SAG type of material uses oxide masks on top of semiconductor wafers to obtain materials with different wavelengths in one single crystal growth. Materials grown in the region with wider oxide coverage, the peak wavelength will shift toward the longer wavelength side. By using different oxide width along the two sides of a waveguide, the material will have different bandgaps along the waveguide. Broadband gain material can thus be achieved. Fig. 52 shows the SAG oxide mask. The widths of the oxide pattern are linearly tapered with a center separation of 14 and 20 ? m. The total taper length is 400 ? m. The grown active material consists of four 2.5 nm thick InGaAsP 1.42 Q wells separated by three 7 nm thick 1.1Q barrier and with two 55 nm thick 1.1 Q optical confinement layers covering the top and bottom. This is the flat region (without oxide). Due to the enhanced growth rate happened in the oxide area, the thickness can be 2-2.5 times higher. A buried heterostructure waveguide is then fabricated inside the SAG region.

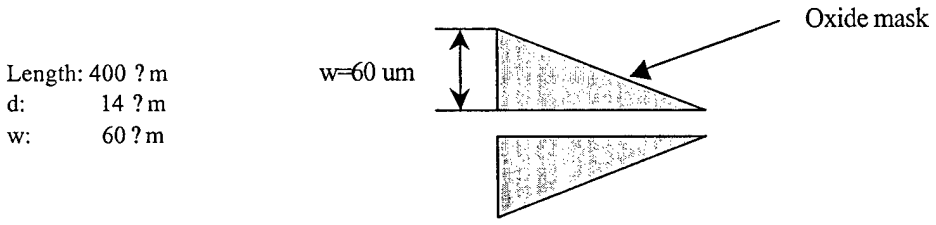


Fig. 52 Oxide masks to grow the SAG gain material

Fig. 53 shows the electro-luminescence (EL) spectrum of a AR-coated SAG waveguide biased at 200 mA. In comparison with it is the EL of a below-threshold 1.3 ? m laser prepared from the same wafer but without the SAG effects. For the SAG material, he gain peak is red-shifted from 1.3 um to around 1.45 um. The measured 10 dB bandwidth is increased from 120 nm to 250 nm. The fabricated laser device is then AR coated from one side and aligned with a 600 groves/mm grating to form a external cavity laser. By rotating the grating we can easily tune the laser. Fig. 54 shows the laser output spectra from an optical spectrum analyzer. The laser can be tuned from around 1.28 ? m to 1.48 ? m. The lasing range is a little bit shifting to the longer wavelength side. We believe that it is because that the longer wavelength materials are pumped by both the injected current and the shorter wavelength photons. Even broader and flatter tuning range should be achieved by using multi-electrodes as well as non-uniform current injection.

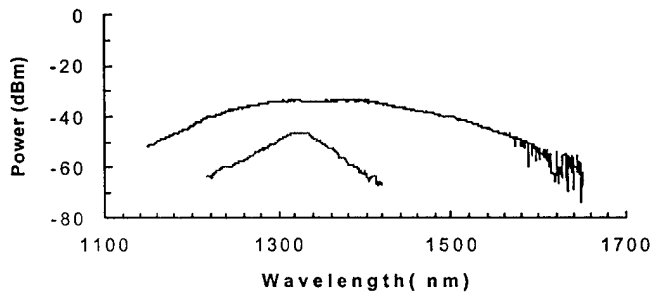


Fig. 53 The electro-luminescence spectrum of a AR-coated SAG waveguide biased at 200 mA. In comparison with it is the EL of a below threshold 1.3 ? m laser.

After a both-side AR coating, we used the device as a wavelength converter. The conversion set up is in the contour-propagating mode where a 1300 nm "DC" laser light is injected from one side and a 1550 nm modulated laser light is injected from the other side. Fig. 54 shows the input 1550 nm signal in the low trace and the output 1300 nm trace in the higher trace. The output is weak at this moment due to the small gain at 1550 nm of the device and due to the non-perfect AR coating, which limited our SOA bias below 120 mA. An optical filter at the output side is also used to pass the 1300 nm signal and reject the back-scattering 1550 nm signal. The filter also contributes some insertion loss. All of these are possible to be improved in the future. Using the nonlinear interaction in a long fiber, Rodney Tucker's group has demonstrated such a wide range wavelength conversion. The device demonstrated widest wavelength conversion range using SOAs.

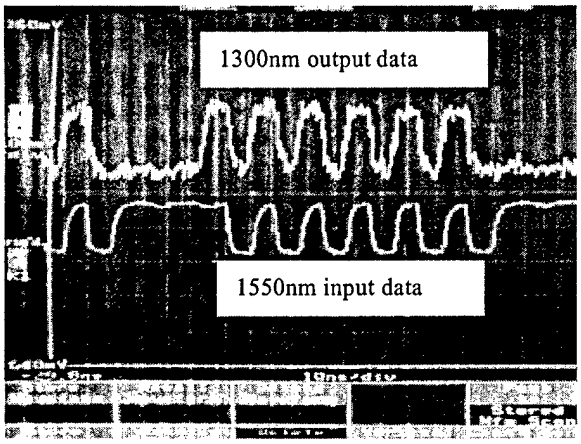


Fig. 54 Wavelength conversion from 1300 nm to 1550 nm,

10. Long Carrier-Lifetime Low-Crosstalk Materials for Switching and Amplifying:

The issues of using semiconductor optical amplifiers (SOAs) as an amplifying material have been their fast gain recovery time. The fast gain recovery time, caused by the short carrier lifetime, produces problems like high channel-crosstalk in a WDM system and high amplified-spontaneous-emission (ASE) noise. In the research work we studied methods to increase carrier lifetime in a broadband SOA. Three different methods were used: a. quasi-indirect bandgap superlattice materials, b. Type II delta-doping materials, and c. SAG exponential gain materials.

a. The Quasi-Indirect Bandgap Superlattice Materials: The materials are composed of multiple layers of direct bandgap and indirect bandgap superlattice materials. For example we can have the GaAs/AlAs (direct/indirect) superlattice on GaAs substrates for shorter wavelength gain materials (700-850 nm) as shown in Fig. 55, and the AlSb/GaSb (indirect/direct) superlattice on GaSb substrates for long wavelength gain materials (1300-1550 nm). Through band mixing of the X-like and the ?-like bands in these superlattices, the composite superlattice bands will have a carrier lifetime somewhere between a direct bandgap material (~ns) and an indirect bandgap material (~?s). The material gain will be reduced accordingly. However, we can increase the device length to increase the gain similar to the EDFA case. In our research work, we have grown

AlAs/GaAs quasi-indirect bandgap superlattice materials and observed materials changing from direct to indirect bandgaps. We grew 2nm/2nm, 5nm/5nm, 8nm/8nm indirect/direct bandgap superlattice materials. We observed that the PL from the 8nm/8nm sample shifted to the shorter wavelength side. We observed much weaker PL signals from the 5nm/5nm sample and shifted to the even shorter wavelength side. We didn't observe any PL from the 2nm/2nm sample. It is believed that the 2nm/2nm sample became an indirect bandgap material. It is highly possible that the carrier lifetime has changed from the nanosecond scale to the microsecond scale with the quasi-indirect bandgap material.

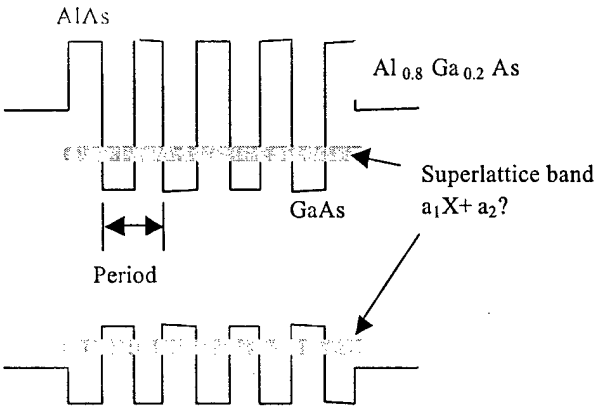


Fig. 55

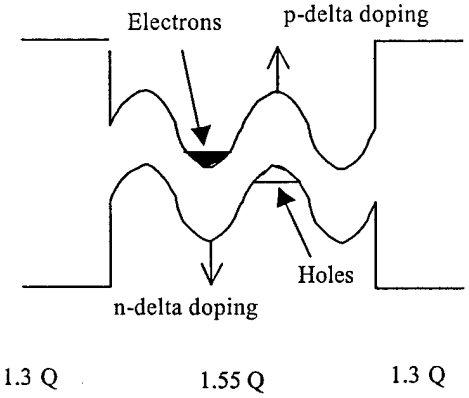
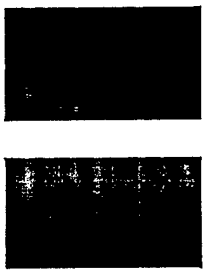


Fig. 56

b. The Type II Delta-Doping Materials: Using multiple layer of n and p delta doping pairs we can create the nipi structure, which can spatially separate the electrons and holes as shown in Fig. 56. Depending on the doping concentration and the separation distance, we can control the carrier recombination lifetime. We have grown hetrostructure gain material with a 100 nm thick 1.3 Q cladding layer on each side and an 80 nm thick 1.55 Q gain layer in the middle. The 1.55 Q material is delta-doped with p and n dopants with a surface concentration of around $5x10^{12}/cm^2$ and a separation of 20 nm. The material shows good PL intensity with a peak shifted to around 1580 nm. It is now sent to another group and waiting for time resolved study results. We expect such a material will have a longer carrier lifetime due to the spatial separation of electrons and holes in the material.

c. The SAG exponential gain materials: The SAG type of material uses oxide masks on top of semiconductor wafers to obtain materials with different wavelengths in one single crystal growth. Materials grown in the region with wider oxide coverage, the peak wavelength will shift toward the longer wavelength side. By using different oxide width along the two sides of a waveguide, as shown in Fig. 57(a), the material will have different bandgaps along the waveguide. In our work, the grown active material consists of four 2.5 nm thick InGaAsP 1.42 Q wells separated by three 7 nm thick 1.1Q barrier and with two 55 nm thick 1.1 Q optical confinement layers covering the top and bottom. A buried heterostructure waveguide is then fabricated inside the SAG region. The SAG type of gain material provides a gain medium with continuously changing bandgap along the waveguide. With a constant current injection, the Fermi level is the same

everywhere along the waveguide, as shown in Fig. 57(b). Since the carrier concentration is exponentially proportional to the difference between the Fermi level and the bandedge, the carrier distribution along the waveguide is exponentially increased from the larger bandgap side to the small bandgap side. If multi-channel WDM signals are injected into the waveguide from the shorter wavelength side, they will see an exponentially increased gain profile along the wavegiude. The optical gain will not saturate in such a case and the crosstalk effect can be reduced.



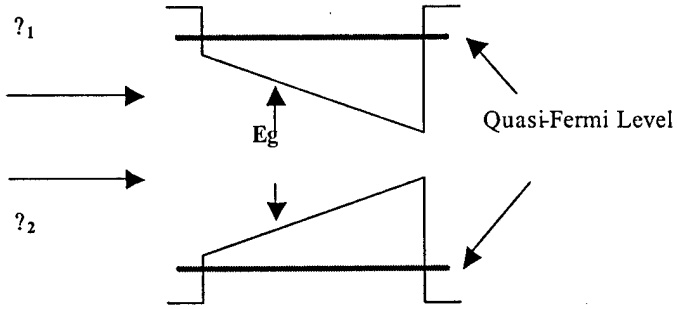
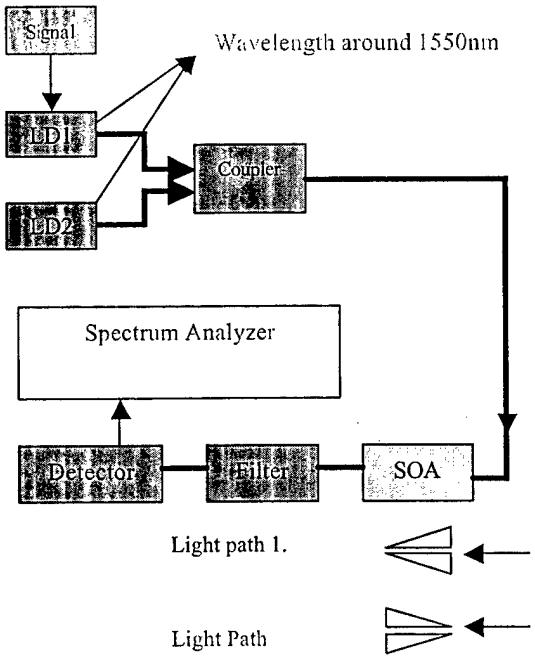


Fig. 57(a)

Fig. 57 (b)



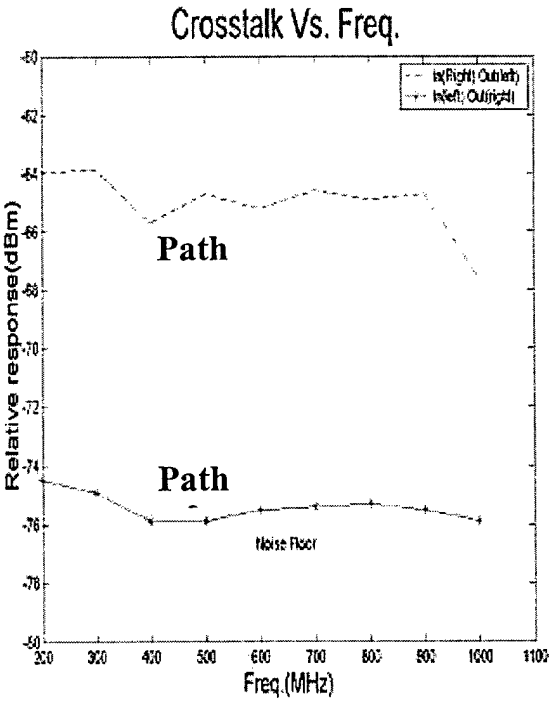


Fig. 58

Fig. 59

The fabricated device has broad gain profile from 1300 nm to 1500nm and is tested using a setup similar to thus we used to do wavelength conversions as shown in Fig. 58. Two transmitter

sources at different wavelengths near 1550 nm are used for pump and probe. We modulate one of the sources with a frequency sweeper. In the receiving side, we connect the filtered detector output to a spectrum analyzer. Fig. 59 shows the measured results. We found, when we propagate signals through the waveguide from the large bandgap side to the small bandgap side, there is no detectable crosstalk among WDM channels. The sweeping curve shows only the noise floor. On the other hand, we observe serious channel crosstalks when we inject WDM signals from the opposite direction. We have also proposed previously that an exponentially decreased gain profile can achieve ultrafast wavelength conversions. The proposed structure can serve as both an ideal optical amplifying material and an ideal wavelength conversion material depending on the signal injection direction.

III. STATUS OF EFFORTS:

At this stage we have completed all our efforts of the "Fabrication and demonstration of a WDM, ATM, Multicast switch" project. We built systems and demonstrated cell delineation, VCI overwriting, and cell synchronization, WDM memory, FPGA route control, and tunable filter cell selection operations at 2.5 Gb/s. We also extended our work to try to obtain very broadband, very low crosstalk gain material to improve our switch scalability. The results are very useful for the construction of near future photonic burst switches and photonic packet switches for NGI and GII applications.

IV. MULTIDISCIPLINARY EDUCATION:

In the course of the research works, there have been many e-mails, phone calls, visits between the two campuses. The interaction among graduate students and postdocs has created a great environment of multidisciplinary discussions and. Many ideas, problem solving discussions, and research papers have been generated through this process. UMBC has graduated 3 M.S. students and 4 Ph. D. students and two more Ph.D students are on the way to graduate. Poly has graduated two Ph. D. students. We have published 12 journal and 62 refereed conference papers and filed 4 patents with two granted in this area. Our works have drawn a great attention from many different equipment vendors and research organizations including NTT optical networking group, Alcatel, CSELT, New Bridge networks, ...etc.. Our constant supporter, Lucent Technology has also shown a great interest in what we are doing. The PI, Prof. Choa, was also visited by Cisco and invited by 3-Com to visit their head quarter and give an invited talk on our photonic packet switching research. We list in the following the project supported personnel, the interaction/transition, and publications as well as patent applications.

Personnel Ever Supported:

1. UMBC:

a. Faculty:

Professor F. S. Paul Choa, Overall project

b. PostDocs:

Dr. X. Wang, (1/2 time) Device Processing
Dr. Y. Chai, (1/2 time) System Experiment
Dr. Y. Zhao (1/2 time) System Experiment
Dr. Z. Chen (new) Device Processing
Dr. Q. Yu (new) System Experiment

c. Graduate Student:

M. S. Students:

B. G. Gopal: (geaduated) is now working at Cadence Semiconductor at CA.
J. Busrur: (graduated) is now working at Bellcore, NJ.
Q. Xiang, (graduated) is now working at Optical Links.

Ph. D. Students:

M. H. Shih: (graduated) worked at SVIC, CA, a cable TV lightwave eqp. He passed away.
J. H. Chen: (graduated) is now working at JDSU, CA. At a new photonis switching branch.
J. Y. Fan: (graduated) is now working at Light-crossing, CA on device design and fabrication.
L. Wang: (graduated) is now working at Agility, CA on system integration.
X Zhao: (To be graduate) system integration
J Zhang (to be graduate) device processing
J Lin (new student), device processing

2. Polytechnic University:

a. Faculty:

Professors H. Jonathan Chao and Haldun Hadimioglu: Electronic control unit, system integration.

b. PostDoc:

Dr. Zhijian Zhang (1/2 time), Sorrento Networks
Dr. Liji Wu. (1/2 time), Internet Photonics

c. Graduate Student:

MS. Students:

Longjun Li, architecture design
Huiping Xiang, system integration

Ph. D. Students:

S. H. Yang, (graduated) Circuit design, TansComm Technology System Inc
T. S. Wang, (graduated) Architecture, Nokia
Guansong Zhang, (current) system integration and architecture design.

Interaction/Transitions:

1. We have been continuously working together with researchers at Lucent Technology to develop photonic switching technologies. Lucent's research executive director, Dr. Bill Brinkman and director, Dr. A. M. Glass have been very interested in the project and discussed with us on it.
2. We have been contacted by 3-Com, CA. about our photonic device capability and photonic switch works. 3-Com is particularly interested in our photonic ATM switches. People in their Israel factory (Fab. ATM switches) has found from the web about our work and 3-com has invited the PI Prof. Choa to visit their research headquarter at San Jose and give an invited talk there.

3. We are also in the process to try to commercialize our photonic devices. Interested parties include Finisar at CA, Cisco at CA. Cisco people also visited UMBC.

Awarded and Pending Patents:

F. S. Choa, "Integrated coherent receiver," U. S. Patent number 5.847.855, Dec. 1998.
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F. S. Choa, "Broadband semiconductor materials for wide-band optical amplifiers and widely tunable lasers," (pending)
F. S. Choa, "A Method to Implement Low-Crosstalk Semiconductor Optical Amplifiers (SOAs), Switches, and/or Gain Materials" (pending)

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12. H.J. Chao, Xiaolei Guo, Cheuk-Hung Lam and Ti-Shiang Wang, "A Terabit IP Switch Router Using Optoelectronic Technology". Invited paper to Journal of High Speed Networks, Vol. 8, p.35-57, April 1999.

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Appendix I. The VHDL Code of the Route Controller

```
library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.std_logic_unsigned.all;

entity router is
    port (
        rst     :       in STD_LOGIC;
        cellclk         :       in STD_LOGIC;
        clk     :       in STD_LOGIC;
        clkn    :       in STD_LOGIC;
        r1, r2 :        in STD_LOGIC;

        wc1, wc2        :       out STD_LOGIC_VECTOR(3 downto 0);
        soa1, soa2      :       out STD_LOGIC_VECTOR(3 downto 0);
        tf1, tf2        :       out STD_LOGIC_VECTOR(3 downto 0)

    );
end router;

architecture router_arch of router is

type FSMstate is (st5, st6, st7, st8, st9, st10, st11, st12);
type OPTstate is (init, ps0, ps1, ps2, st1, st2, st3, st4, st5, st6);

component wavefifo
        port (
        din: IN std_logic_VECTOR(1 downto 0);
        wr_en: IN std_logic;
        wr_clk: IN std_logic;
        rd_en: IN std_logic;
        rd_clk: IN std_logic;
        ainit: IN std_logic;
        dout: OUT std_logic_VECTOR(1 downto 0);
        full: OUT std_logic;
        empty: OUT std_logic);
end component;

signal dly_cellclk1     : STD_LOGIC;
signal dly_cellclk2     : STD_LOGIC;
signal startup          : STD_LOGIC;

signal iw_din   : STD_LOGIC_VECTOR(1 downto 0);
signal iw_dout : STD_LOGIC_VECTOR(1 downto 0);
signal iw_wen   : STD_LOGIC;
signal iw_ren   : STD_LOGIC;
signal iw_empty         : STD_LOGIC;
signal iw_full : STD_LOGIC;

signal ow1_din : STD_LOGIC_VECTOR(1 downto 0);
signal ow1_dout         : STD_LOGIC_VECTOR(1 downto 0);
signal ow1_wen : STD_LOGIC;
signal ow1_ren : STD_LOGIC;
signal ow1_empty: STD_LOGIC;
signal ow1_full         : STD_LOGIC;

signal ow2_din : STD_LOGIC_VECTOR(1 downto 0);
signal ow2_dout         : STD_LOGIC_VECTOR(1 downto 0);
signal ow2_wen : STD_LOGIC;
signal ow2_ren : STD_LOGIC;
signal ow2_empty: STD_LOGIC;
signal ow2_full         : STD_LOGIC;

signal curstate         : FSMstate;
signal outstate         : OPTstate;
signal initcntr         : STD_LOGIC;
```

```
signal wlth1   : STD_LOGIC_VECTOR(1 downto 0);
signal wlth2   : STD_LOGIC_VECTOR(1 downto 0);
signal owlth1  : STD_LOGIC_VECTOR(1 downto 0);
signal owlth2  : STD_LOGIC_VECTOR(1 downto 0);

signal wc1_sel : STD_LOGIC_VECTOR(2 downto 0);
signal wc2_sel : STD_LOGIC_VECTOR(2 downto 0);
signal soa1_sel : STD_LOGIC_VECTOR(3 downto 0);
signal soa2_sel : STD_LOGIC_VECTOR(3 downto 0);
signal tf1_sel : STD_LOGIC_VECTOR(2 downto 0);
signal tf2_sel : STD_LOGIC_VECTOR(2 downto 0);

signal outempty1       : STD_LOGIC;
signal outempty2       : STD_LOGIC;
signal wvlempty1       : STD_LOGIC;
signal wvlempty2       : STD_LOGIC;

signal soa1_sel1: STD_LOGIC_VECTOR(3 downto 0);
signal soa2_sel1: STD_LOGIC_VECTOR(3 downto 0);
signal soa1_sel2: STD_LOGIC_VECTOR(3 downto 0);
signal soa2_sel2: STD_LOGIC_VECTOR(3 downto 0);

signal wc1a, wc2a      : STD_LOGIC_VECTOR(3 downto 0);
signal tf1a, tf2a      : STD_LOGIC_VECTOR(3 downto 0);

begin

idle_wavelength_fifo : wavefifo
               port map (
                       din => iw_din,
                       wr_en => iw_wen,
                       wr_clk => clkn,
                       rd_en => iw_ren,
                       rd_clk => clkn,
                       ainit => rst,
                       dout => iw_dout,
                       full => iw_full,
                       empty => iw_empty);

output1_wavelength_fifo : wavefifo
               port map (
                       din => ow1_din,
                       wr_en => ow1_wen,
                       wr_clk => clkn,
                       rd_en => ow1_ren,
                       rd_clk => clkn,
                       ainit => rst,
                       dout => ow1_dout,
                       full => ow1_full,
                       empty => ow1_empty);

output2_wavelength_fifo : wavefifo
               port map (
                       din => ow2_din,
                       wr_en => ow2_wen,
                       wr_clk => clkn,
                       rd_en => ow2_ren,
                       rd_clk => clkn,
                       ainit => rst,
                       dout => ow2_dout,
                       full => ow2_full,
                       empty => ow2_empty);


process(rst, clkn)
begin
  if ( rst = '1' ) then
    dly_cellclk1 <= '0';
    dly_cellclk2 <= '0';
  elsif ( clkn'event and clkn = '1' ) then
```

```
    dly_cellclk1 <= not cellclk;
    dly_cellclk2 <= dly_cellclk1;
  end if;
end process;

startup <= cellclk and dly_cellclk2;

process(rst, clk)
begin
  if ( rst = '1' ) then
    iw_ren <= '0';
    ow1_wen <= '0';
    ow2_wen <= '0';

    wc1_sel <= "100";
    wc2_sel <= "100";

    curstate <= st5;

  elsif ( clk'event and clk = '1' ) then

      case curstate is
        when st5 =>
          if ( startup = '1' and initcntr = '1' ) then
            if ( iw_empty = '1') then
              wc1_sel <= "100";
              wc2_sel <= "100";
              curstate <= st11;
            else
              wvlempty1 <= '0';
              iw_ren <= '1';
              curstate <= st6;
            end if;
          else
            curstate <= st5;
          end if;

        when st6=>
          iw_ren <= '0';
          wlth1 <= iw_dout;
          curstate <= st12;

        when st12 =>
          if ( iw_empty = '0' ) then
            iw_ren <= '1';
            wvlempty2 <= '0';
          else
            iw_ren <= '0';
            wvlempty2 <= '1';
            wc2_sel <= "100";
          end if;
          curstate <= st7;

        when st7 =>
          if ( wvlempty2 = '0' ) then
            iw_ren <= '0';
            wlth2 <= iw_dout;
          end if;

          if ( wvlempty1 = '0' ) then
            if ( r1 = '0' ) then
              ow1_wen <= '1';
              ow1_din <= wlth1;
            else
              ow2_wen <= '1';
              ow2_din <= wlth1;
            end if;
          end if;
          curstate <= st8;

        when st8 =>
```

```
            if ( wvlempty1 = '0' ) then
              wc1_sel <= '0'&wlth1;
            else
              wc1_sel <= "100";
            end if;

            if ( wvlempty2 = '0' ) then
              wc2_sel <= '0'&wlth2;
            else
              wc2_sel <= "100";
            end if;

            if ( wvlempty1 = '0' ) then
              if ( r1 = '0' ) then
                ow1_wen <= '0';
              else
                ow2_wen <= '0';
              end if;
            end if;
            curstate <= st9;

          when st9 =>
            if ( wvlempty2 = '0' ) then
              if ( r2 = '0' ) then
                ow1_wen <= '1';
                ow1_din <= wlth2;
              else
                ow2_wen <= '1';
                ow2_din <= wlth2;
              end if;
            end if;
            curstate <= st10;

          when st10 =>
            if ( wvlempty2 = '0' ) then
              if ( r2 = '0' ) then
                ow1_wen <= '0';
              else
                ow2_wen <= '0';
              end if;
            end if;
            curstate <= st5;

          when st11 =>
            if ( startup = '0' ) then
              curstate <= st5;
            else
              curstate <= st11;
            end if;

        end case;
    end if;
end process;

process(rst, clk)
begin
    if ( rst = '1' ) then
      soa1_sel <= "1111";
      soa2_sel <= "0000";
      tf1_sel <= "100";
      tf2_sel <= "100";

      iw_wen <= '0';
      ow1_ren <= '0';
      ow2_ren <= '0';

      outstate <= ps0;
      initcntr <= '0';

    elsif ( clk'event and clk = '1' ) then
      case outstate is
```

```
    when ps0 =>
      iw_wen <= '1';
      iw_din <= "00";
      outstate <= ps1;

    when ps1 =>
      iw_wen <= '1';
      iw_din <= "01";
      outstate <= ps2;

    when ps2 =>
      iw_wen <= '0';
      initcntr <= '1';
      outstate <= init;

when init =>
  if ( startup = '1' ) then

    if ( ow1_empty = '0') then
      outempty1 <= '0';
      ow1_ren <= '1';
    else
      outempty1 <= '1';
      ow1_ren <= '0';
    end if;
    if ( ow2_empty = '0') then
      outempty2 <= '0';
      ow2_ren <= '1';
    else
      outempty2 <= '1';
      ow2_ren <= '0';
    end if;
    outstate <= st1;
  else
    outstate <= init;
  end if;

when st1 =>
  if ( outempty1 = '0' ) then
    ow1_ren <= '0';
    owlth1 <= ow1_dout;
  end if;
  if ( outempty2 = '0' ) then
    ow2_ren <= '0';
    owlth2 <= ow2_dout;
  end if;
  outstate <= st2;

when st2 =>
  if ( outempty1 = '0' ) then
    tf1_sel <= '0'&owlth1;
  else
    tf1_sel <= "100";
  end if;

  if ( outempty2 = '0' ) then
    tf2_sel <= '0'&owlth2;
  else
    tf2_sel <= "100";
  end if;
  outstate <= st6;

when st6 =>
  if ( outempty1 = '0' ) then
    if ( outempty2 = '0' ) then
      soa1_sel <= soa1_sel1 and soa1_sel2;
      soa2_sel <= soa2_sel1 or soa2_sel2;
    else
      soa1_sel <= soa1_sel1;
      soa2_sel <= soa2_sel1;
```

```
        end if;
      else
        if ( outempty2 = '0' ) then
          soa1_sel <= soa1_sel2;
          soa2_sel <= soa2_sel2;
        else
          soa1_sel <= "1111";
          soa2_sel <= "0000";
        end if;
      end if;
      outstate <= st3;

    when st3 =>
      if ( outempty1 = '0' ) then
        iw_wen <= '1';
        iw_din <= owlth1;
      else
        iw_wen <= '0';
      end if;
      outstate <= st4;

    when st4 =>
      if ( outempty2 = '0' ) then
        iw_wen <= '1';
        iw_din <= owlth2;
      else
        iw_wen <= '0';
      end if;
      outstate <= st5;

    when st5 =>
      iw_wen <= '0';
      outstate <= init;

  end case;
 end if;

end process;

soa1_sel1 <= "1110" when tf1_sel = "000" else
             "1101" when tf1_sel = "001" else
             "1011" when tf1_sel = "010" else
             "0111" when tf1_sel = "011" else
             "1111";

soa2_sel1 <= "0001" when tf1_sel = "000" else
             "0010" when tf1_sel = "001" else
             "0100" when tf1_sel = "010" else
             "1000" when tf1_sel = "011" else
             "0000";

soa1_sel2 <= "1110" when tf2_sel = "000" else
             "1101" when tf2_sel = "001" else
             "1011" when tf2_sel = "010" else
             "0111" when tf2_sel = "011" else
             "1111";

soa2_sel2 <= "0001" when tf2_sel = "000" else
             "0010" when tf2_sel = "001" else
             "0100" when tf2_sel = "010" else
             "1000" when tf2_sel = "011" else
             "0000";

wc1a <= "0001" when wc1_sel = "000" else
        "0010" when wc1_sel = "001" else
        "0100" when wc1_sel = "010" else
        "1000" when wc1_sel = "011" else
        "0000";

wc2a <= "0001" when wc2_sel = "000" else
        "0010" when wc2_sel = "001" else
```

```
        "0100" when wc2_sel = "010" else
        "1000" when wc2_sel = "011" else
        "0000";

tf1a <= "0001" when tf1_sel = "000" else
        "0010" when tf1_sel = "001" else
        "0100" when tf1_sel = "010" else
        "1000" when tf1_sel = "011" else
        "0000";

tf2a <= "0001" when tf2_sel = "000" else
        "0010" when tf2_sel = "001" else
        "0100" when tf2_sel = "010" else
        "1000" when tf2_sel = "011" else
        "0000";

process(rst, cellclk)
begin
  if ( rst = '1' ) then
    wc1 <= "0000";
    wc2 <= "0000";
    soa1 <= "1111";
    soa2 <= "0000";
    tf1 <= "0000";
    tf2 <= "0000";

  elsif ( cellclk'event and cellclk = '1' ) then
    wc1 <= wc1a;
    wc2 <= wc2a;
    soa1 <= soa1_sel;
    soa2 <= soa2_sel;
    tf1 <= tf1a;
    tf2 <= tf2a;
  end if;
end process;

end router_arch;
```

Appendix II.

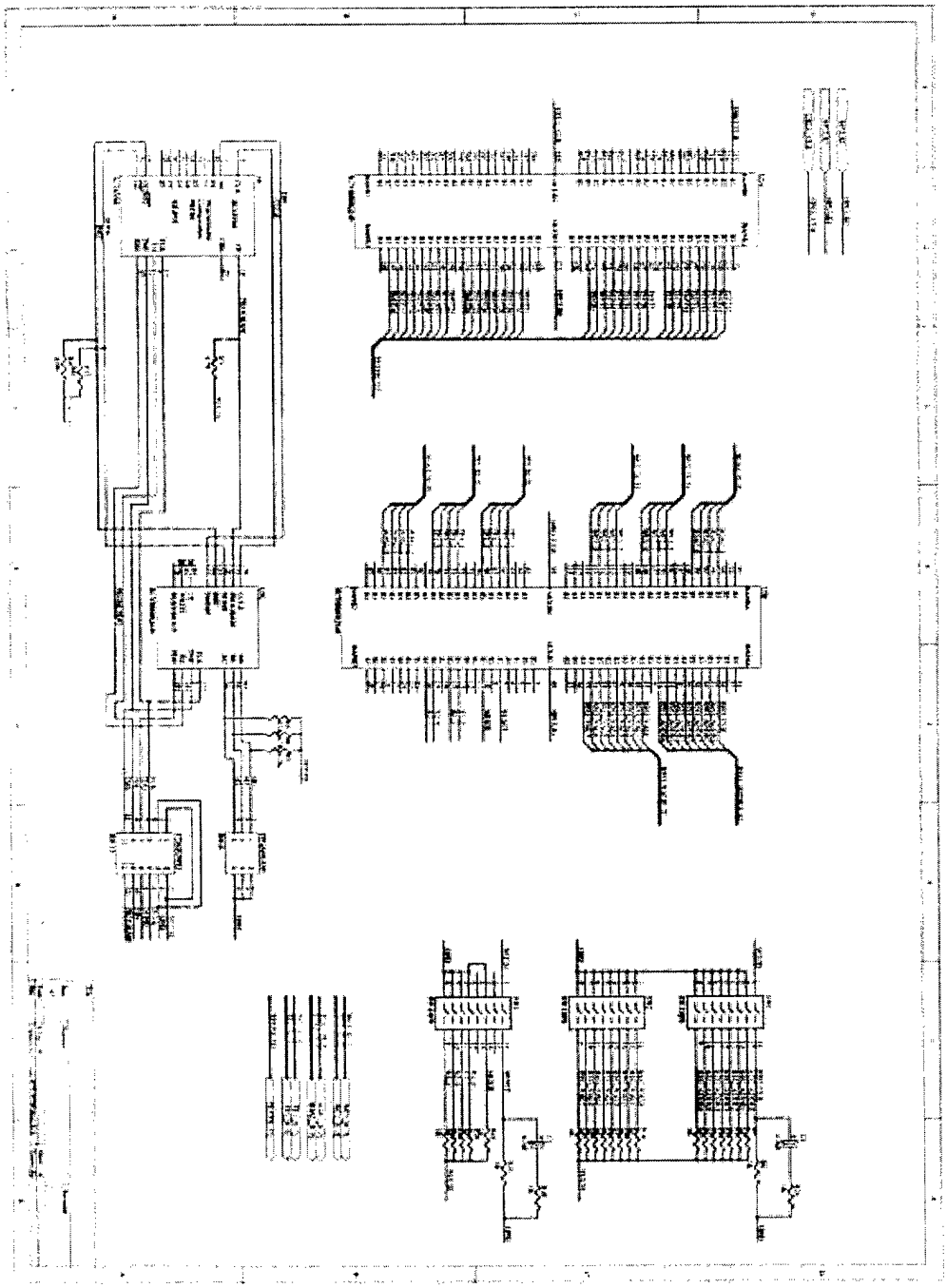

Figure 1. The FPGA subcircuit of the Route Controller.

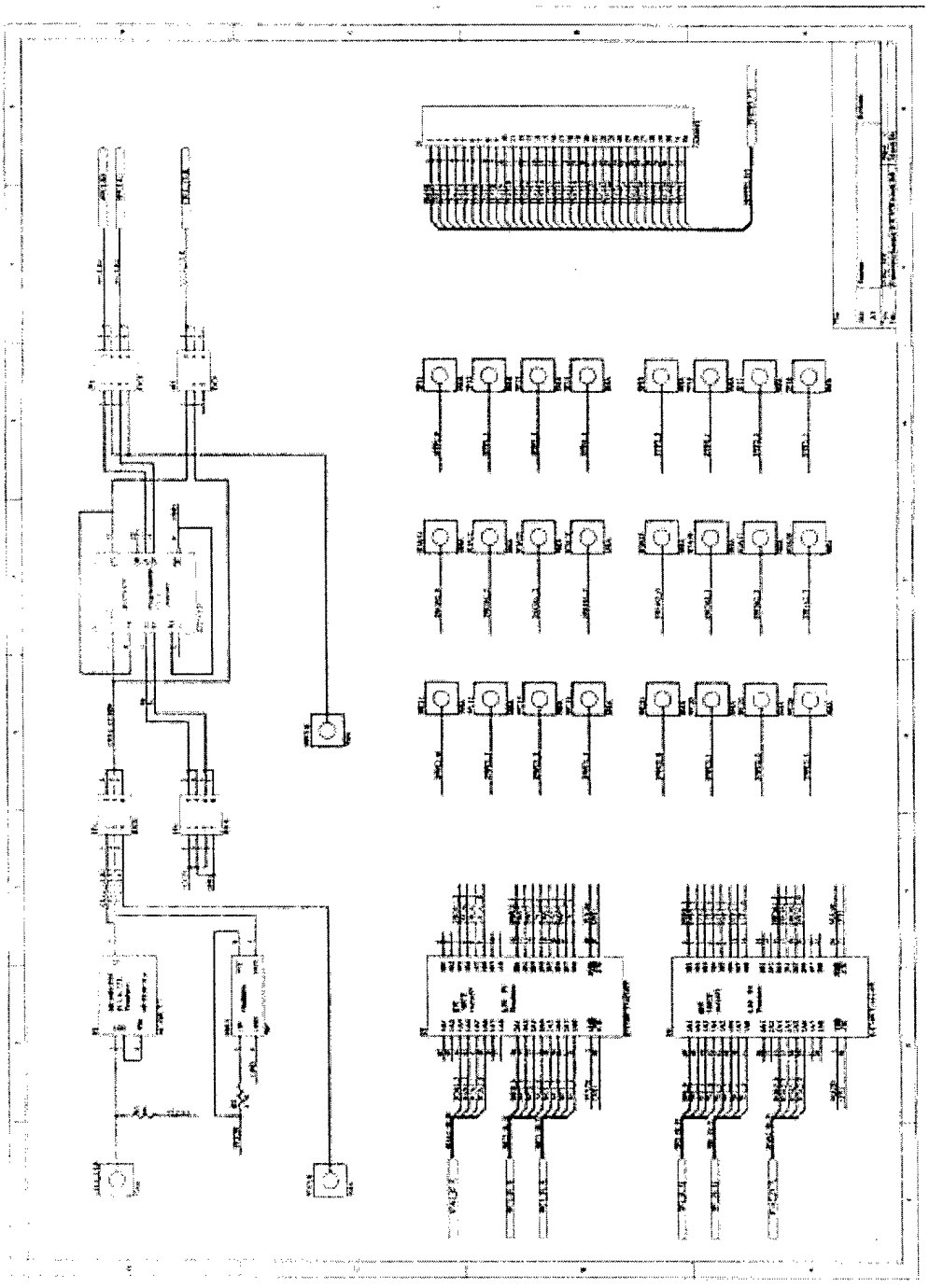

Figure 2. The Clock Subcircuit of the Route Controller.

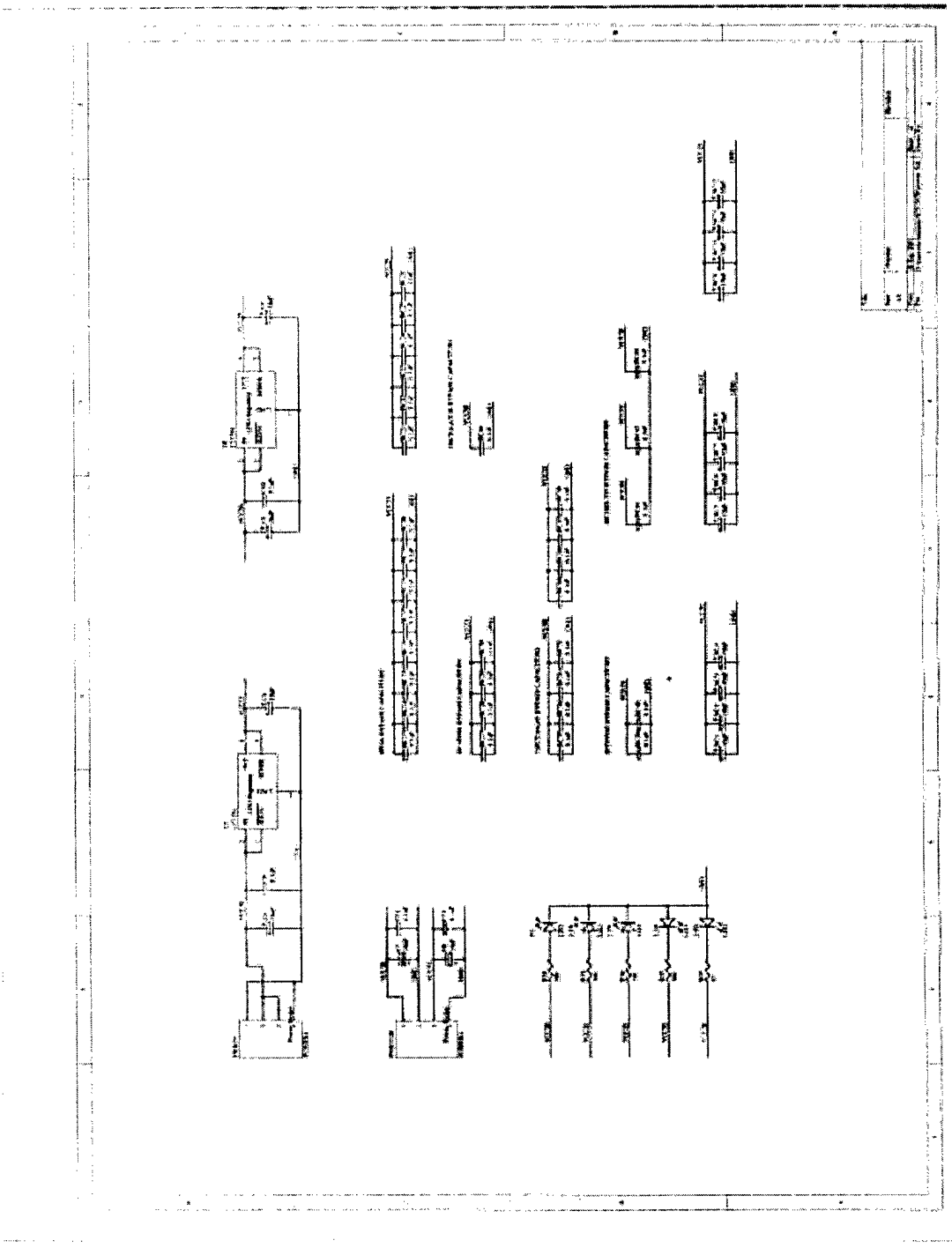

Figure 3. The Power Subcircuit of the Route Controller.

Veon Wendy Civ AFRL/AFOSR

From: Fow-sen Choa [choa@umbc.edu]
Sent: Wednesday, July 10, 2002 3:23 PM
To: pkcontracting@afosr.af.mil
Cc: Alexis Nathan
Subject: Final Report


Untitled


Untitled


Untitled


Untitled


Untitled

Dear Contract Manager(s):

This is to respond to your letter on June 3rd, 2002 to UMCP ORA. Attached are our final report and invention reports. A hard copy of the final report and a CD copy of its full Word document have been sent to the AFOSR program manager. In the letter it is also mentioned that we have to send the patent report to AFOSR/AJ. Can you let us know their address? Or they have a email address we can send the 4 page invention report to them? Thanks!

Prof. Fow-Sen Choa
UMBC
410-455-3272 (O)